Instruction Manual
40-385.4A
V2.10

MDAR
Relay System

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MDAR Relay System

(V2.10)

MDAR REVISION NOTICE

DATE	REV LEVEL	PAGES REMOVED	PAGES INSERTED
11/92	Released		
9/94	A	ii, v, vi, vii, viii, & ix	same
		2-11	2-11 & 12
		3-2, 6, & 9	same
		4-8, 17	same
		5-8	same
		A-1, 2, 4, & 5	same
		B-1, 2, 3, & 4	same
		C-1, 4, 5, 6, & 7	same
		D-1, 2, & 4	same
		E-1, 4, 8, & 10	same
		F-1, 4	same
		G-1, 3, 4, 5, 6, & 7	same
		H-1, 3, & H-13, 14,	same
		Index-1 to 6	same
		J-1 to J-5	same

CHANGE SUMMARY:

A CHANGE BAR (▌) LOCATED IN THE MARGIN REPRESENTS A TECHNICAL CHANGE TO THE PRODUCT.

It is recommended that the user of MDAR equipment become acquainted with the information in this instruction leaflet before energizing the system. Failure to do so may result in injury to personnel or damage to the equipment, and may affect the equipment warranty. If the MDAR relay system is mounted in a cabinet, the cabinet must be bolted to the floor, or otherwise secured before MDAR installation, to prevent the system from tipping over.

All integrated circuits used on the modules are sensitive and can be damaged by the discharge of static electricity. Electrostatic discharge precautions should be observed when handling modules or individual components.

ABB does not assume liability arising out of the application or use of any product or circuit described herein. ABB reserves the right to make changes to any products herein to improve reliability, function or design. Specifications and information herein are subject to change without notice. All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding a particular installation, operation or maintenance of equipment, the local ABB representative should be contacted.

PREFACE

Scope

This manual describes the functions and features of the MDAR Relay System. It is intended primarily for use by engineers and technicians involved in the installation, testing, operation and maintenance of the MDAR system.

Equipment Identification

The MDAR equipment is identified by the Catalog Number on the MDAR chassis nameplate. The Catalog Number can be decoded by using Catalog Number Table 3-1 (see Section 3).

Production Changes

When engineering and production changes are made to the MDAR equipment, a revision notation (SUB #) is reflected on the appropriate schematic diagram, and associated parts information. A summary of all Sub #s for the particular release is shown below.

Equipment Repair

Repair work is done most satisfactorily at the factory. When returning equipment, carefully pack modules and other units, etc. All equipment should be returned in the original packing containers if possible. Any damage due to improperly packed items will be charged to the customer.

Document Overview

The circuitry is divided into 6 standard modules and one option module. Section 1 provides the Product Description, which includes software functions. [Appendices A through G include related module circuit descriptions.] Section 2 presents the Specifications. Section 3 presents Pilot and Non-Pilot applications with related Catalog Numbers for ordering purposes. MDAR Installation, Operation and Maintenance are described in Section 4, with related Setting Calculations in Section 5. Acceptance Tests for both Non-Pilot and Pilot System are described in Appendix H. Appendix I shows Index to Nomenclature. System Diagrams are included in Appendix J.

Contents of Relay System

The MDAR Relay System includes the style numbers, listed below, with appropriate sub numbers (representing revision levels) for each module. Addenda pages may be included (representing future revisions).

Module	Style and Sub Number
• Backplane	1609C23-13
(Sub-Backplane Xfmr)	1498B70-3
• Interconnect	1611C30-9
• Option	1608C39-6
• Filter	1608C38-9
• Microprocessor	1611C14-7
• Display	1609C01-4
• Power Supply	1608C35-16

Software System

MDAR software version V2.10 is included in this I.L.

Setting Nomenclature Appliques

If this I.L. is included as part of the shipment of an MDAR Relay system, the I.L. will contain setting nomenclature appliques which can be placed in a convenient location, e.g., inside the two FT-14 covers. The appliques provide a convenient (and complete) set of MDAR “settings” (see Table 4-1 for setting nomenclature). There are two appliques which are printed protective sheets (contained in a plastic envelope); the back of the sheets can be removed thereby exposing a stick-on surface.

Features Included in Version V2.10

The following features are ***standard*** for the Non-Pilot MDAR V2.10:

- 3-Zone phase and ground distance relay, with reversible Zone 3 phase and ground; 4 impedance units per zone: 3 phase-to-ground; 1 phase-to-phase.
- Selectable Zone 1 extension
- Zone 1 timer (0 or 2 cycles)
- Independent timers for phase and ground (T2G, T2P, T3G, T3P)
- Inverse time directional or non-directional (selectable) ground overcurrent backup logic
- Loss of potential supervision (LOP)
- Loss of current monitoring (LOI)
- Overcurrent supervision of phase and ground distance
- Instantaneous forward directional phase and ground highset overcurrent trip (ITP and ITG)
- Close Into Fault Trip (CIFT)
- Stub Bus Protection (89b)
- Unequal-pole-closing load pickup logic
- Selectable Loss-of-Load accelerated trip logic
- Current change fault detector (ΔI)
- Voltage change fault detector (ΔV)
- Line voltage, current and phase angle monitor.
- Last Fault LED blinks once for a single fault and twice for more than one fault. When the RESET button is depressed, the flashing LED is reset, and the displayed data is returned to the Volts/Amps/Angle...metering mode. MDAR fault data memory cannot be cleared from the front panel. Fault data can be accessed by selecting Last Fault or Previous Fault Display Mode
- Selectable polarizing for directional O/C ground units (ZSEQ/NSEQ/DUAL)
- Programmable Reclose initiation and reclose block (RB) outputs; Reclose Initiate (RI2) can be enabled with the selection of:
  - 1PR for ϕG fault
  - 2PR for ϕG or $\phi\phi$ fault
  - 3PR for ϕG or $\phi\phi$ fault or 3ϕ fault
- Numerical (Digital) Processing
- Fault locator
- Self-checking software with Failure Alarm and Displayed error codes
- Push-to-close test for output contacts
- Software switches for functional tests, e.g., TK (SEND), RS1, RS2 and RS12 (Receivers).
- Trip contact sealed by trip current, with selectable dropout delay timer, 0/50 ms
- Real-time clock
- 16 fault record storage with selectable capture mode
- 16 sets of oscillographic data and intermediate target data. Each set includes 7 analog graphic inputs and 24 digital intermediate targets with 8 samples per cycle. Each analog input contains 1 prefault and 7 fault cycles
- Selectable oscillographic data capture setting trip, Z2PU, Z2Z3 or ΔV/ΔI
- Selectable Data Capture Setting (FDAT) - TRIP, Z2PU/TRIP, Z2Z3/TRIP
- Logic for load restrictions
- • Selectable phase sequence rotation of ABC or ACB
- Out-of-Step block logic

NOTE: The foregoing (and following) features preceded by two dots (• •) were not included in V2.02.

Features Included in Version V2.10

The following features are ***standard*** for the Pilot MDAR V2.10:

- All features listed as standard for the Non-Pilot MDAR V2.10 are included in the Pilot system
- Independent pilot phase and ground distance units
- Complete Logic and Channel Interface for:
  - Permissive Overreach Transfer Trip (POTT) / Simplified Unblocking
  - Permissive Underreach Transfer Trip (PUTT)
  - Directional Comparison Blocking Scheme (BLK)
  - POTT or Simplified Unblocking Weakfeed
- Instantaneous Forward Directional Overcurrent Function for High Resistance Ground Fault Supplement to Overreach Pilot, with adjustable timer (from 0 to 15) in 1 cycle steps or Block
- Instantaneous Reverse Directional Overcurrent Ground Function
  - Carrier Ground Start on Blocking Scheme
  - Weakfeed System Application
- Reclose Block on Breaker Failure (BF) Squelch
- 3-Terminal Line Application
- Weakfeed Trip

Features Included in Version V2.10

The following features are ***optional*** for the Non-Pilot ***and*** the Pilot MDAR V2.10:

- Choice of rear communications port options:

  RS232C/PONI or

  INCOM®/PONI
- Optional graphic software program (OSCAR)
- Built-in FT-14 test switches
- • Optional Programmable Output Contacts. Eight additional contacts chosen from 30 functions
- Single-Pole-Trip (SPT) logic and outputs:
  - SPT/RI1 on first ϕGF and 3PT on other fault types
  - 3PT/RB if reclosing on a permanent fault
  - 3PT/RB if second phase(s) fault during single phasing
  - 3PT on a time delay limit (o.35-5.0 sec in 0.05 sec steps) if the system fails to reclose (62T).
- Setting options for TRIP/Reclose Initiate (RI) mode selector:

TTYP SET AT	TRIP	RI
OFF	3PT	NO
1PR	3PT	RI2 (ϕG)
2PR	3PT	RI2 (ϕG, ϕϕG)
3PR	3PT	RI2 (ϕG, Mϕ)
SPR	SPT (ϕG)	RI1
	3PT (Mϕ)	N0
SR3R	SPT (ϕG)	RI1
	3PT (Mϕ)	RI2

SPT = Single Pole Trip

3PT = 3 Pole Trip

RI = Reclose Initiate

RB = Reclose Block

RI2 = 3 Pole Reclose Initiate

RI1 = Single Pole Reclose Initiate

ϕG = Single Phase-to-Ground Faults

Mϕ = Multi-Phase Faults

ϕϕ = 2-Phase Faults

NOTE: The foregoing (and following) features preceded by two dots (• •) were not included in V2.02.

Significant Changes to V2.10 (from V2.02)

(For customers who are familiar with Version 2.00 and beyond)

1. Add an O/C supervision (Im) for Phase faults (AND-2, AND-4, AND-6 & AND-191) and OST (AND-131C & AND-122). Remove IL supervision from AND-131C & AND-122).
2. Change PT setting range from 300-7000 to 100-7000 with 5 per steps.
3. Modify 52b control circuit by adding an AND-3C to supervise Z1G (AND-3A) and FDOG (AND-188) trip. For V2.02, the ground units will not trip if the breaker is open, e.g., 52b = 125 volts.
4. Modify SPT logic by adding OR75B and changing the input of OR78J from X2 to X2A (0/50). For version 2.02, the MDAR relay will not trip after single pole reclosing on a permanent SPF if the setting of LV is very low because the LV setting supervises the ROF tripping.
5. Add eight programmable contact outputs with two programmable timers which can be set for pickup and dropout from 0 to 5 seconds with 0.01 sec per steps.
6. Selectable ABC or ACB phase rotation by jumper #3. The rotation is shown on the Metering mode.

   NOTE: For rotation ABC, jumper #3 on the Microprocessor Module should be removed.
7. Change the input of AND-120 from the switch of PLT to BLK. The STOP contact should be operated only for the Blocking system.
8. Add a display saver routine. The MDAR display will be on for 5 minutes after turning the dc power on, depressing any one of the front panel pushbuttons or detecting faults on the line.
9. Change front target display from “IN” to “IP” and add two readings “$3I_0$”and “$\angle 3I_0$” to the fault target display.

NOTE: CONVERSION FROM MDAR FIRMWARE VERSION V2.0x TO V2.10 CAN BE ACCOMPLISHED AS FOLLOWS:

1. Standard precautions of static voltage discharges should be observed such as using a grounded wrist strap when handling Integrated Circuits.
2. Remove chips U103, U104, and U202 from the Microprocessor module.
3. Replace chips U103 (G11) and U104 (G12) and U202 into the sockets.
4. Check Jumper #3 on Microprocessor module for rotation ABC or ACB system which is shown on the Metering mode. Normally, JMP3 should be “OUT” for ABC system. Spare jumpers should be placed on locations JMP10, 11 or 12. Remove any spare jumper (JMP10, 11 or 12) and replace it to JMP3 position for ACB system.
5. Check Jumper #2 on Microprocessor module. Position 2-3 is used for single-pole trip logic only and position 1-2 is used for three-pole trip or programmable output contact logic.
6. Reprogram MDAR password through INCOM® remote communication.
7. It is recommended to verify the relay’s operation per Section 2 of Appendix H (Acceptance/Maintenance Tests).

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Section 1. PRODUCT DESCRIPTION

1.1 INTRODUCTION

The MDAR relay assembly (**Figure 1-1**) is a numerical transmission line protection system, with three zones of distance protection. All measurements and logic are performed by digital means, using a microprocessor. Self-checking and line monitoring techniques are included. *MDAR is primarily recommended for application on non-series compensated lines.*

The non-pilot MDAR relay system is standard (**see Section 3**); an optional pilot MDAR relay system is also available (in **Section 3**).

1.2 MDAR CONSTRUCTION

The standard nomenclature for **ABB** relay protection equipment is as follows:

- Cabinet - contains fixed-racks, swing-racks, or open racks
- Rack - contains one or more chassis (e.g., the MDAR)
- Chassis - contains several modules (e.g., Microprocessor or Power Supply)
- Module - contains a number of functional circuits (on printed circuit board)
- Circuit - a complete function on a printed circuit board (e.g., analog-to-digital conversion)
- The MDAR relay assembly consists of an outer-chassis and an inner-chassis which slides into the outer-chassis. The MDAR conforms to the following dimensions and weight (**see also Section 2**):
  - Height 7" (requires 4 rack units; 1.75" each)
  - Width 19"
  - Depth 13.6"
  - Weight 35 Lbs

All of the relay circuitry, with the exception of the input isolation transformers and first-line surge protection, are mounted on the inner chassis, to which the front panel is attached. The outer chassis has a Backplate, which is a receptacle for all external connections, including a communication adaptor (**see Figure 4-1**). Two FT-14 switches may be included, as options, in the two peripheral areas of the outer chassis. The FT-14 switches permit convenient and safe disconnection of trip, ac and dc input circuits, and provide for injection of test signals.

The MDAR relay provides the following contact outputs:

- 4 make contacts (2 **TRIP**, 2 **BFI**); 8 additional optional contacts when Single-pole Trip option is used
- Single-pole Reclose Initiate (2 Form A)
- Three-pole Reclose Initiate (2 Form A)
- Reclose Block (2 Form A)
- General Start (1 Form A)
- System Failure Alarm (1 Form C)
- TRIP Alarm (1Form C; 1 Form A is available if SBP is not used)
- 8 additional programmable contacts when the Contact module is used

1.3 MDAR MODULES

The inner and outer chassis, together, contain 6 standard modules, plus the option module for single pole trip applications (**see Figure 1-2**). The Backplate is connected to the Backplane module (outer chassis). The remaining modules are attached to the inner chassis:

- Interconnect module
- Option module or Contact module
- Filter module
- Microprocessor module
- Display module
- Power Supply module

Circuit descriptions for each module, may be found in **Appendices A thru G**, in accordance with the list in the Preface to this document (**see** "**Contents of Relay System**").

1.3.1 Backplane Module

The Backplane Assembly includes three voltage transformers, four current transformers, two filter chokes and several surge protection capacitors.

The Backplane Module (**see Appendix A**) receives all external connections (with or without the FT-14 switch option), and connects directly to the Interconnect module, thru plug-in connectors (J11, J12, J13)

which provide the connection between outer and inner chassis.

The female parts of the connectors are mounted on the Backplane module, which is part of the outer chassis. The male parts of the connectors are mounted on the Interconnect module, which is part of the inner chassis.

The INCOM® or RS232C PONI[1] (**see Figure 1-3**) is mounted on the backplate of the outer chassis and is connected to the Backplane module.

1.3.2 Interconnect Module

The Interconnect module (**see Appendix B**) becomes the floor of the MDAR inner chassis; it provides electrical connections from and to all other modules: from the Backplane (at the rear), to the Filter and Power Supply modules (at left and right, respectively), and to the Microprocessor and Display modules at the front of the inner chassis.

The Interconnect module receives inputs V_{AN}, V_{BN}, V_{CN}, I_A, I_B, I_C, I_P from the Backplane module and feeds them to the Filter module. The I_P input is used for zero-sequence dual-polarizing ground current measurement; the input is from the power transformer neutral ct. Also, seven opto-couplers, on the Interconnect module, send the following signals to the Microprocessor module:

- **External Reset** - resets the front target display.
- **52b** - used for close-into-fault (**CIF**) detection, load loss trip (**LLT**) and carrier-start and stop control in a pilot system.
- **52a** (for single-pole trip option; i.e., for pole disagreement).
- **Pilot Enable** - should be “ON” for the pilot system option.
- **Receiver #1** (for Pilot option) - carrier receiver for two terminal application.
- **Receiver #2** (for Pilot option) - second carrier receiver for three-terminal application.
- **SBP (89b)** for stub bus protection.

1.3.3 Option Module/Contact Module

For single-pole tripping applications, an Option module (**see Appendix C**) is added with extra tripping and reed relays. The Option module plugs into the Interconnect module.

For 3-pole tripping application, an optional Contact module can be plugged into the connector and provide 8 additional programmable output contacts.

1.3.4 Filter Module

The Filter module (**see Appendix D**) band-limits the seven inputs from the Interconnect module: V_{AN}, V_{BN}, V_{CN}, I_A, I_B, I_C, I_P. These inputs are fed to the Microprocessor module (analog signal multiplexer).

1.3.5 Microprocessor Module

The Microprocessor module (**see Appendix E**) includes the following subsystems:

- **Microprocessor** - Intel 80C196, a 16-bit microcontroller operating with a 10 MHz clock.
- **EPROM** - Program memory in separate, easily-replaced EPROM chips.
- **PROM** - Programmable read-only memory.
- **RAM** - Volatile read-write memory, for working storage.
- **NOVRAM (EEPROM)** - Non-volatile memory for storing settings and fault-data targets when the MDAR relay is deenergized.
- **A/D Converter** - The seven inputs from the Filter module are analog-multiplexed to a single sample/hold circuit. The output of the sample/hold is fed to the Analog-to-Digital Converter through an auto-ranging circuit which shifts gain by a factor of eight.
- **Digital I/O Circuitry** - Status inputs from breaker auxiliary contacts (**52a** and **52b**), and external reset signal are interfaced to the microprocessor via optical isolators (**Figure 4-2**). The microprocessor executes control outputs using dry contacts. Output relays (**Figure 4-2**) are used for breaker tripping, breaker failure initiation (**BFI**), reclose initiation (**RI**), and reclose blocking (**RB**). General start contact (**GS**) is provided for starting the external sequence of events or fault recorders. Trip and relay-failure alarm contacts are included. Reed relays in the trip circuits sense trip coil current flow and feedback target information to the microprocessor.

For the option of Contact module, eight additional output contacts are provided and can be programmed from 30 functions shown in **Table 3-4**.

1. *“INCOM “stands for INtegrated COMmunications. The “*PONI*” acronym stands for Product Operated Network Interface.*

NOTE: JMP3 should be "OUT" for normal ABC rotation. Insert a jumper into JMP3 position for ACB phase rotation system application.

1.3.6 Display Module

The Display module has two (four-digit) alphanumeric displays for settings, metering fault designation and information. The metering display shows three-phase voltage, current and angle. Fault data, stored in the Microprocessor module, is accessible through the front panel display. Fault data includes: pre-fault phase A voltage, current and angle. It also shows the type of fault, fault voltages, currents, angles and fault location. The Display module is attached to the front panel (**see Figure 1-1**); it can be used to access and store data, and contains 7 LEDs, as follows:

- Relay in Service (ready to use)
- Settings (can read or change settings)
- Volts/Amps/Angles (can read measuring inputs)
- Last Fault (when flashing, indicates new fault information available)
- Previous Fault (when last fault LED flashes twice/minute, indicates information for the fault preceding the last fault)
- Value Accepted (when the Settings LED is also "ON", a new setting value is accepted; when the Test LED is also "ON", the output contacts can be tested)
- Test (can verify self-check and perform functional test)

The display will be blocked momentarily, every minute, for the purpose of self-check; this will not affect the relay protection function.

A display saver software is also built in. The MDAR display will be on only for 5 minutes after turning the dc power on or depressing any one of the front panel pushbuttons or detecting faults on the line.

1.3.7 Power Supply Module

The Power Supply module (**see Appendix G**) is available in three ranges:

- 38 - 70 Vdc
- 88 - 145 Vdc
- 176 - 290 Vdc

Provides isolation from station battery; includes overcurrent and overvoltage protection. Status monitoring and loss-of-power indication are accomplished via a failure-alarm relay (on the Interconnect module). Relay is normally picked up, but the processor deenergizes it when a problem is found. Total power loss also drops-out the relay. Front-panel test points provide access to power-supply output voltages for test purposes:

- +12 Vdc
- -12Vdc
- -24 Vdc
- + 5 Vdc

1.3.8 Contact Outputs

1.4 TEST ACCESSORIES

The MDAR may be tested with two devices:

- Inner Chassis Test Fixture.

This device is similar to the outer chassis, and includes a Backplane and Transformer assembly.

- Extender Board

This device includes two small pc boards with two ribbon cables. The inner chassis can be tested outside of the outer case by means of the Extender Board.

1.5 FAULT DETECTION SOFTWARE

MDAR fault-detection software operates in two modes:

- Background mode
- Fault mode

The MDAR relay normally operates in the "Background mode" where it looks for phase current or phase voltage disturbances. Once a phase disturbance is detected, the relay enters the "Fault mode". During non-fault operation (in the Background mode), the MDAR Microprocessor (U100) used its spare time to check its hardware, service the operator panel, and check for a disturbance in voltage or current which indicates a possible fault. If a disturbance is seen, the programs switch to the Fault mode, for several power cycles or longer, to perform phase and ground unit checks for each zone and function.

1.5.1 Background Mode

During the background mode, the seven inputs (currents and voltages shown in **Figure 1-4**) are sampled to test for line faults. These currents and voltages are sampled and converted into digital quantities and input to the Microprocessor where all signal processing takes place. (MDAR detects faults

by digital computation; not by analog.) The system continuously takes 8 samples per cycle. The components of the signals which are power system frequency are extracted.

The MDAR software which does the sampling has 8 states; these states correspond to the sampling rate (8 samples per cycle). Movement from state to state is controlled by a timer. The timer is loaded with a state time at the beginning of the state. The code executed within a state should be completed before the timer expires. The software then waits for the timer to time out.

The MDAR relay program functions are included in a flow chart loop (shown in **Figure 1-5**), which the Microprocessor repeats 8 times per power cycle. Most functions are performed all of the time, in the background mode, as shown. An important detail (not shown in **Figure 1-5**) is that many of the checks are broken into small parcels, so that the whole complement of tasks is performed over a one-cycle period (eight passes through the loop). Some of the checks are performed more than once per cycle.

The 60 Hz components are extracted from the samples (from each cycle) and converted to voltage and current phasor values using a Fourier notch-filter algorithm. An additional dc-offset correction algorithm reduces overreach errors from decaying exponential transients. During the process, the sum of squares of the inputs are accumulated to provide rms values of current and voltage. The Fourier coefficients and sums are calculated for computing the phase angles. The sum of squares and the sums of the Fourier coefficients are updated for each sample, using information from the previous seven samples, to provide a full cycle of data.

1.5.2 Fault Mode and Restricted Fault Tests

Upon entry into the fault mode, the sums of the Fourier coefficients and sum of squares from the background mode are stored. New sums are obtained, using fault data, to which offset compensation has been applied.

To speed up tripping for severe faults, restricted fault testing is implemented. The last half cycle of background mode input samples and the first half cycle of fault mode input samples are used to compute the current and voltage vectors and rms values. No dc offset compensation is performed. High-set instantaneous overcurrent and Zone 1 distance unit tests are executed (**see Section 3.2**, MDAR Line Measurement). This will speed up tripping by as much as one cycle for high current faults.

Instantaneous overcurrent, inverse time overcurrent protection, and out-of-step blocking are also conducted during the fault mode and background mode.

For Zone-2 and Zone-3 faults (**see Section 3**), impedance computation and checking will continue throughout the specified time delay. The impedance calculation will be performed once every cycle, in the fault mode and background mode.

1.5.3 Unique Qualities of MDAR

A unique characteristic of the MDAR system is its phase selection principle. It determines the sum of positive and negative sequence currents for each phase by a novel method which excludes the influence of pre-fault load current. From this information, the fault type can be clearly identified and the actual distance to the fault can be estimated.

High-resistance ground-fault detection is available in MDAR. Sensitive directional pilot tripping is achieved through an **FDOG** timer (**FDGT**), which is selectable from 0 to 15 cycles or block, on the Microprocessor module. The pilot distance unit is always active and has the priority for tripping.

Load-loss tripping entails high-speed, essentially simultaneous clearing at both terminals of a transmission line for all fault types except three-phase, without the need of a pilot channel.

Any fault location on the protected circuit will be within the reach of the zone 1 relays at one or both terminals. This causes direct tripping of the local breaker without the need for any information from the remote terminal. The remote terminal recognizes the loss of load-current in the unfaulted phase(s) as evidence of tripping of the remote breaker. This, coupled with Zone-2 distance or directional overcurrent ground fault recognition at that terminal, allows immediate tripping to take place at that terminal.

1.6 SELF-CHECKING SOFTWARE

MDAR continually monitors its ac input subsystems using multiple A/D converter calibration-check inputs, plus loss-of-potential and loss-of-current monitoring described. Failures of the converter, or any problem in a single ac channel which unbalances nonfault inputs, trigger alarms. Self-checking software includes the following functions:

a. Digital Front-end A/D Converter Check

b. Program Memory Check Sum

Immediately upon power-up, the relay does a complete **ROM** (**EPROM**) checksum of program memory. Afterwards, the MDAR relay continually computes the program memory checksum.

c. Power Up **RAM** Check

Immediately upon power-up, the relay does a complete **ROM** test of the **RAM** data memory.

d. Nonvolatile **RAM** Check

All front-panel-entered constants (settings) are stored in nonvolatile **RAM** in three identical arrays. These arrays are continuously checked by the program. If all three array entrees disagree, a nonvolatile **RAM** failure is detected.

For failures which do not disable the processor, the cause of the problem can be read on the display.

The failure modes, represented by their corresponding bits (zero thru 5), are shown in the value field if the “Test” mode is selected by the “Display Select” pushbutton.

- Bit 0 External RAM Failure
- Bit 1 EEPROM Warning
- Bit 2 ROM (EPROM) Failure
- Bit 3 EEPROM Failure (Non-Volatile memory)
- Bit 4 Analog Input Circuit Failure
- Bit 5 Microprocessor Failure
- Bit 6 Setting Discrepancy

All bits are expressed in a HEX byte form. For example, if the display shows “Test 1B”, whose binary representation is 00011011, this means that the relay failed the self-test in the area of External RAM (bit 0), EEPROM (one-out-of-three failure, bit 1), EEPROM (two-out-of-three failure, bit 3) and Analog Input Circuit (bit 4). Normally, the test mode should show “Test 0", meaning that the relay passed the self-test routines.

Bit 6 is for the setting discrepancy detection. If the ordering information calls for single-pole trip option and the jumper #2 on Microprocessor module is on position “1-2”, which is for the programmable output contacts, the MDAR will give the error of “TEST 40".

1.7 UNIQUE REMOTE COMMUNICATION (WRELCOM®) PROGRAM

Two optional types of remote interface can be ordered.

- RS232C - for single point computer communication.
- INCOM® - for local network communication.

A special software (WRELCOM®) program is provided for obtaining or sending the setting information to the MDAR. The MDAR front panel shows two fault events (last and previous), but thru the remote communication, 16 fault events and 16 records of intermediate target data can be obtained and stored. Each record of the intermediate target data contains 8-cycle information (1-prefault and 7 post-fault), with 7 analog inputs and 24 digital data (at the sampling rate of 8 per cycle). Refer to WRELCOM® manual for detailed information.

1.8 POWER SYSTEM ROTATION ABC OR ACB SELECTION

The phase rotation ABC or ACB can be selected by a jumper #3 on the Microprocessor module. The system indicates ABC rotation without jumper #3. With jumper #3 in place, the input phase sequence should be ACB, e.g., phase A leads phase C, C leads B and B leads A, respectively. The rotation is shown on the Metering Mode.

⚠ WARNING

Check jumper #3 before energizing the relay. Normally, it should be removed for phase sequence rotation ABC.

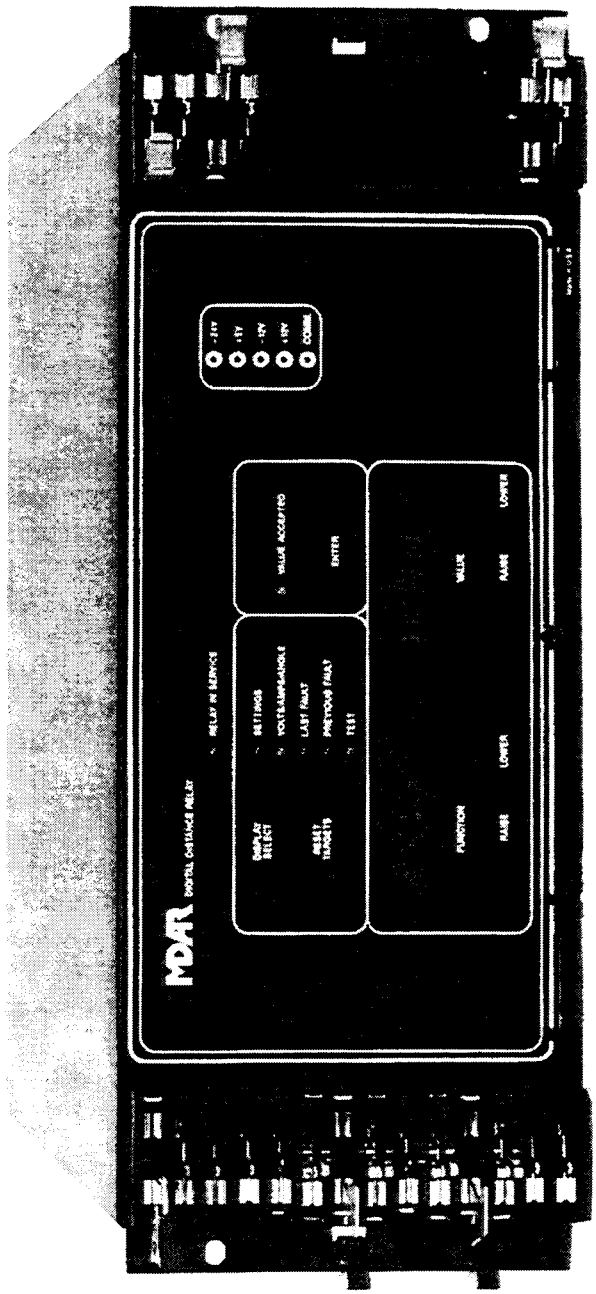


Figure 1-1 MDAR Relay Front Panel

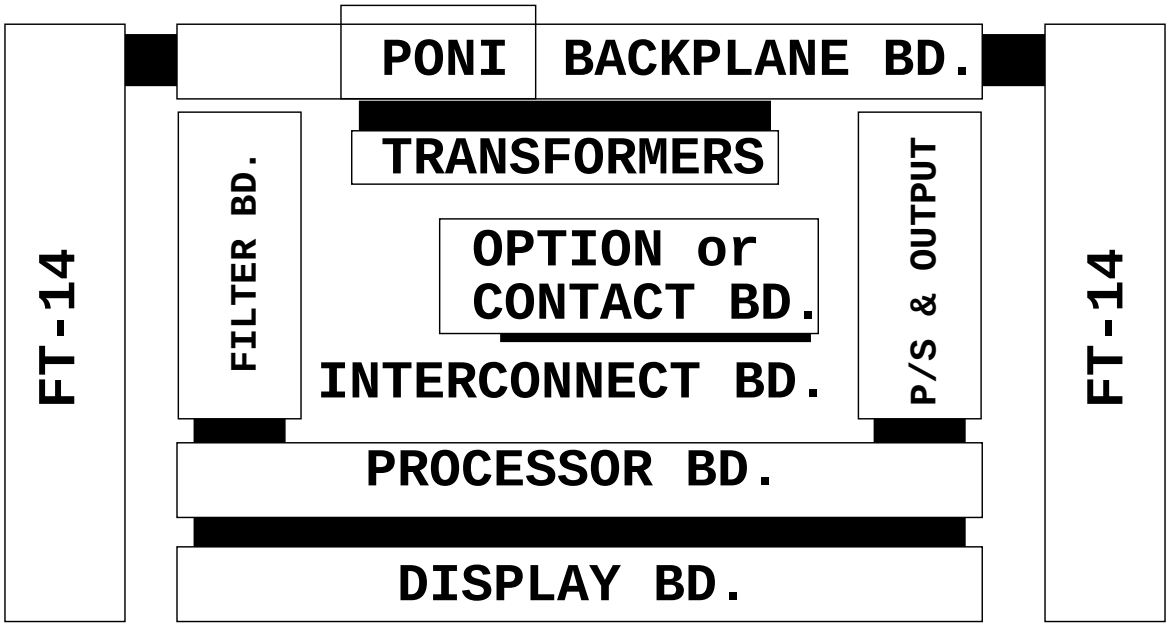


Figure 1-2 Layout of MDAR Modules Within Inner and Outer Chassis

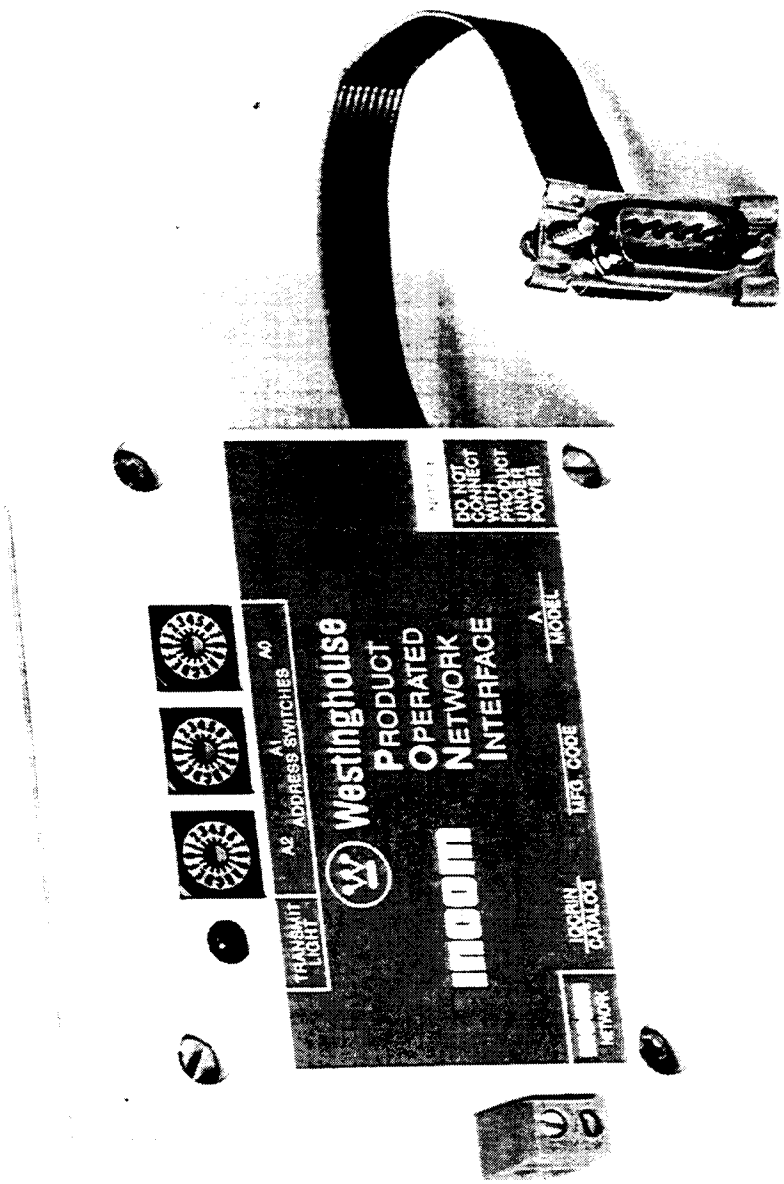


Figure 1-3 INCOM®/PONI Communication Interface Device

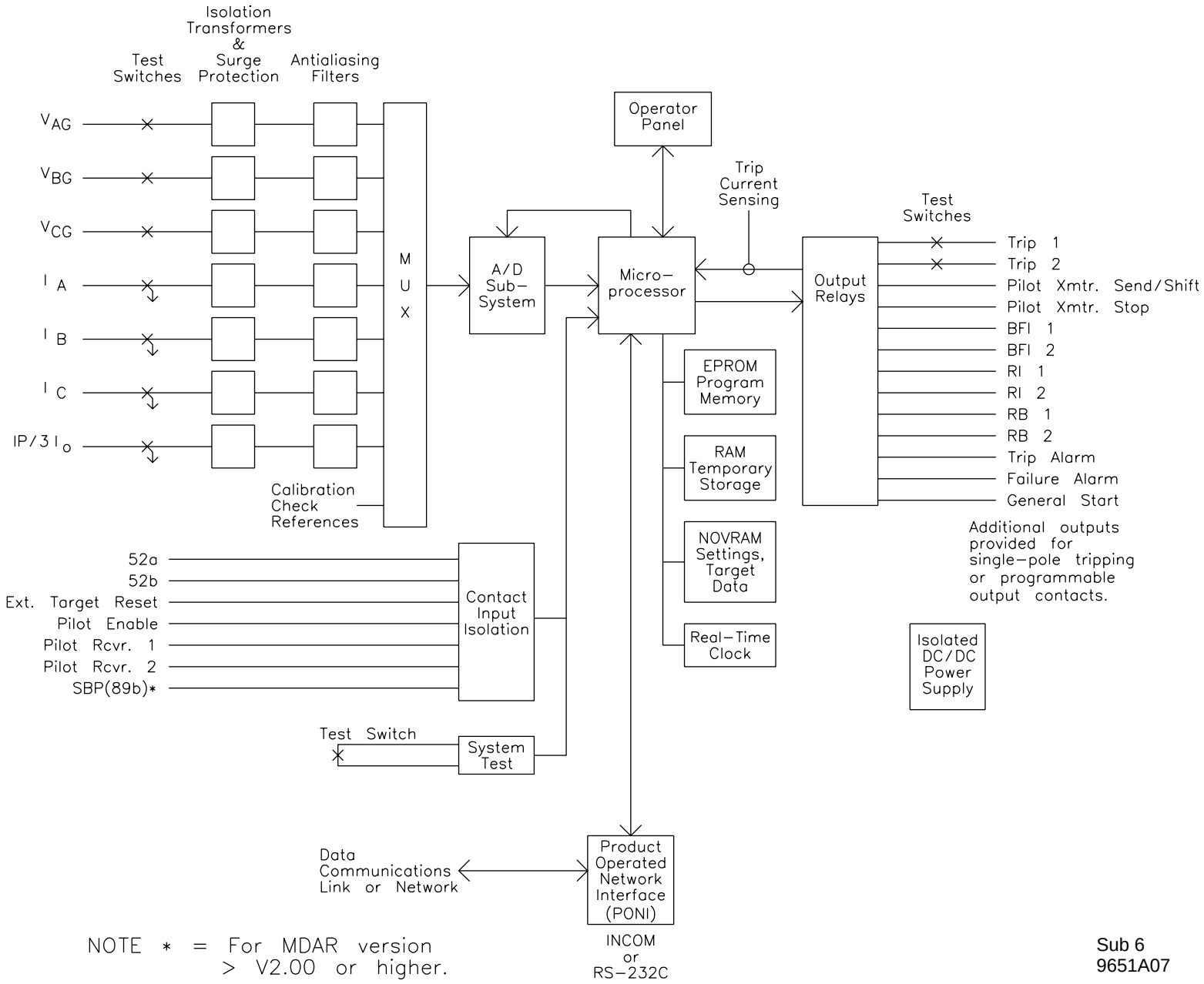


Figure 1-4 Simplified Block Diagram of MDAR Relay

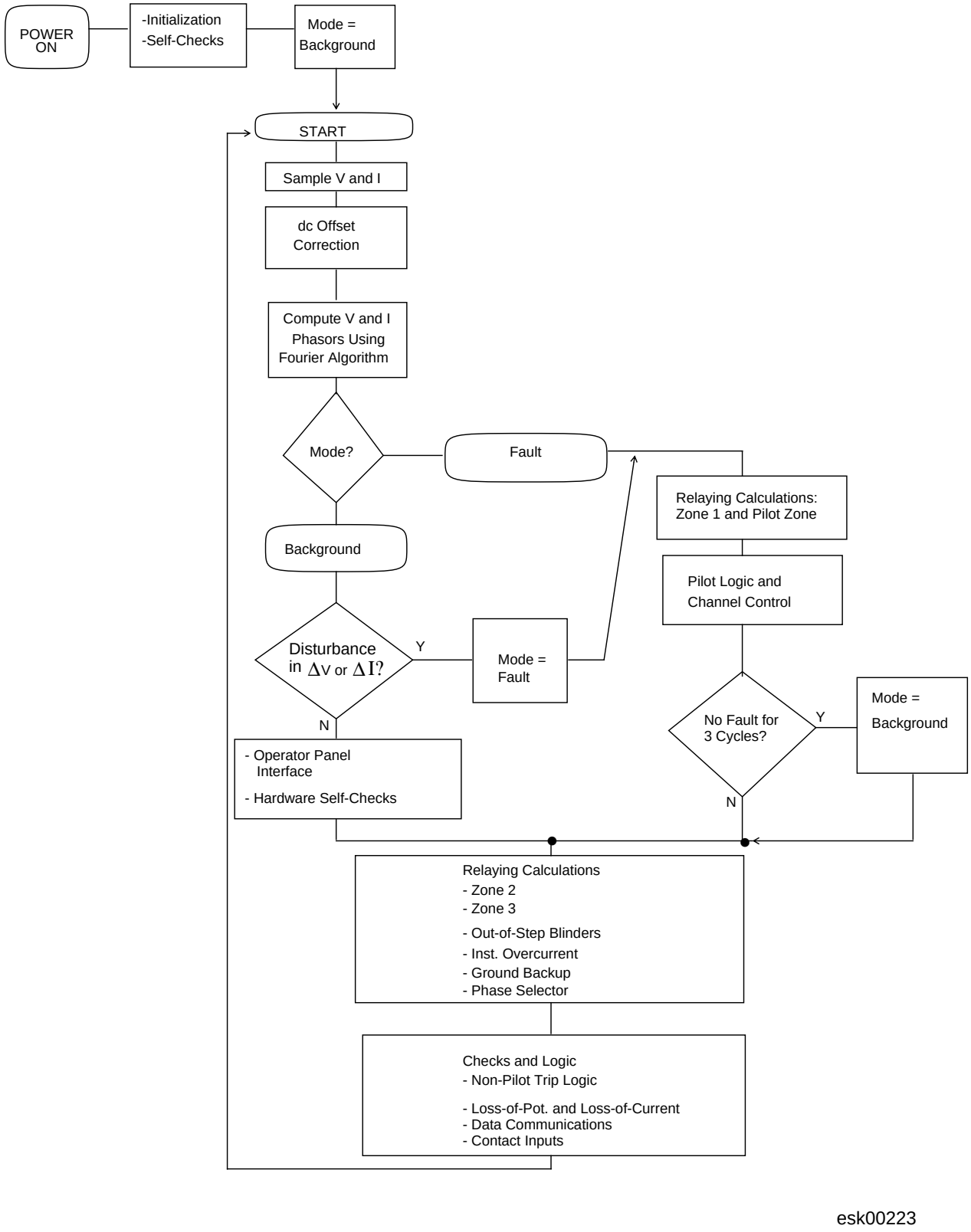


Figure 1-5 MDAR Relay Program Functions

Section 2. SPECIFICATIONS

2.1 TECHNICAL

Operating Speed (from fault detection to trip contact close -60 Hz)	12-14 ms (minimum) 22 ms (typical)
ac Voltage (VLN) at 60 Hz (VLN) at 50 Hz	70 Vrms 63.5 Vrms
ac Current (In)	1 or 5 A
Rated Frequency	50 or 60 Hz
Maximum Permissible ac Voltage	
• Continuous	1.5 x nominal voltage
• 10 Second	2.5 x nominal voltage
Maximum Permissible ac Current	
• Continuous	3 x Nominal Current
• 1 Second	100 x Nominal Current
Typical Operating Current	0.5 A
dc Battery Voltages	

Nominal	Operating Range
48/60 Vdc	38 - 70 Vdc
110/125 Vdc	88- 145 Vdc
220/250 Vdc	176 - 290 Vdc

dc Burdens: Battery	7 W normal 30 W tripping
ac Burdens:	
Volts per Phase	0.02VA at 70 Vac
Current per Phase	0.15VA at 5 A

2.2 EXTERNAL CONNECTIONS

Terminal blocks located on the rear of the chassis suitable for #14 square tongue lugs

Wiring to FT-14 switches suitable for #12 wire lugs

2.3 CONTACT DATA

Trip Contacts - make & carry 30 A for 1 second, 10 A continuous capability, break 50 watts resistive or 25 watts with L/R =.045 seconds

- Non-Trip Contacts
  1A Continuous
  0.1A Resistive Interrupt Capability

Supports 1000 Vac across open contacts

Contacts also meet IEC - 255-6A, IEC - 255-12, IEC -255-16, BS142-1982.

2.4 MEASUREMENTS

Number of zones: 3 zones are standard (optional pilot adds additional zone).

Operating Characteristics: variable mho characteristics for all fault types.

2.5 MEASUREMENT UNITS

Three variable mho phase-to-earth units and one variable mho phase-to-phase impedance unit per zone.

One ground directional (ITG) and one phase directional (ITP) high-set overcurrent unit.

Three-phase non-directional overcurrent units (IL) for load loss trip and CIFT.

One non-directional phase overcurrent unit medium set (Im) for phase supervision.

One non-directional ground overcurrent unit medium set (IOM) for ground supervision.

One ground overcurrent unit for LOI monitoring.

One inverse time overcurrent ground unit with CO characteristics (**see Figures 2-1 thru 2-7**); selectable non-directional or directional capability.

One forward set instantaneous directional overcurrent ground unit. (Pilot-high resistance ground faults.)

Three under-voltage units (LV) for weakfeed and LOP supervision.

Four current change fault detectors, and three voltage change fault detectors.

One instantaneous overcurrent unit low set (IOS)

One reverse set instantaneous directional overcurrent ground unit (Pilot Carrier Start, Weakfeed, Transient Blocking)

2.6 SETTING RANGES

Phase and Ground Distance (Zone 1, 2, 3):

- 0.01-50 ohms in 0.01 ohm steps for 5 A (ct)
- 0.05-250 ohms in 0.05 ohm steps for 1 A (ct)

Zone Timers - Separate timers for phase and ground:

- Zone-1 (No/Yes; 2 cycle delay if Yes is selected)
- Zone-2 (0.10 to 2.99 seconds in 0.01 second steps, Block)
- Zone-3 (0.10 to 9.99 seconds in 0.01 second steps, Block)

Forward Directional Ground Timer (FDGT)

- 0 to 15 cycles in 1 cycle steps, Block

Ohms per Unit Distance

- 0.300-1.500 in 0.001/DTYP (Km or Mi)

Inverse Time Overcurrent Ground Relay:

- Pickup (0.1-0.8) in 0.1 A increments for 1 A (ct).
- Pickup (0.5-4.0) in 0.5 A increments for 5A (ct). Choice of 7 time-curve families (CO-2, 5, 6, 7, 8, 9, 11 Characteristics), 63 time curves per family. (**See Figures 2-1 thru 2-7.**)
- Set for directional or non-directional operation.

High set instantaneous directional overcurrent trip units - phase and ground (I_{AH}, I_{BH}, I_{CH}, I_{OH}).

- 2.0-150 in 0.5 A steps for 5 A (ct)
- 0.4-30 in 0.1 A steps for 1 A (ct)

2.7 GROUND/ PHASE OVERCURRENTS AND UNDERVOLTAGE UNITS

- Undervoltage level units (LVA, LVB, LVC and CIF) for weakfeed and close-into-fault, from 40 to 60 Vrms in 1-volt steps.
- Current Units (IAL, IBL, ICL, IOS, IOM & IM)
  0.5 - 10 in 0.5 A steps for 5 A (ct)
  0.1 - 2 in 0.1 A steps for 1 A (ct)

Current Change Fault Detectors (ΔI_A,ΔI_B,ΔI_C, and ΔI_0), no setting required.

Voltage change fault detectors (ΔV_A, ΔV_B and ΔV_C) no setting required

Ground Overvoltage Unit $3V_0$ (no setting required).

2.8 OPTIONAL SINGLE-POLE-TRIP LOGIC AND OUTPUTS (Without Programmable Contact Option)

- SPT/RI1 on first ϕGF fault and 3PT on other types of faults
- 3PT/RB if reclosing on a permanent fault
- 3PT/RB if second phase(s) fault during single phasing
- 3PT on a selectable time delay limit if the system fails to reclose (62T)
- TRIP/RI mode selections (TTYP):

SELECT	TRIP	RI
OFF	3PT	NO
1PR	3PT	RI2(ϕG)
2PR	3PT	RI2(ϕG,ϕϕ)
3PR	3PT	RI2(ϕG,ϕϕ,Mϕ)
SPR	SPT (ϕG)	RI1
	3PT (Mϕ)	NO
SPR/3PR	SPT (ϕG)	RI1
	3PT (Mϕ)	RI2

Legend:

SPT - Single Pole Trip
3PT - 3-Pole Trip
RI - Reclose Initiation
RB - Reclose Block
RI2 - 3-Pole Reclose Initiate
RI1 - Single Pole Reclose Initiate
ϕG - Single Phase to Ground Faults
Mϕ - Multi-Phase Faults
ϕϕ - 2-Phase Faults

2.9 OPTIONAL PROGRAMMABLE OUTPUT CONTACTS (Without Single-pole Trip Option)

Eight programmable contacts selected from 30 pre-assigned signals which can be programmed either AND or OR logic together. (**Refer to Table 3-4** for the 30 signals.)

- Four NO heavy duty contacts with FT-switches and 1 timer for pickup and/or dropout delay (0 to 5 sec. in 0.01 steps)
- Four Standard contacts with jumper selection for NO or NC outputs and one timer for pickup and/or dropout delay. (0 to 5 sec. in 0.01 sec/step).

2.10 OUT-OF-STEP BLOCK

- OSB Override Timer
  400-4000 ms in 16 ms steps
- OSB Inner Blinder (RT)
  1.0-15.0 ohms in 0.1 ohm steps

NOTE: The RT is a standard setting; for load restriction.

- OSB Outer Blinder (RU)
  3.0-15.0 ohms in 0.1 ohm steps

2.11 SELECTABLE PHASE SEQUENCE ABC OR ACB ROTATION

A jumper #3 on Microprocessor module is used for phase rotation selection.

- ABC system – without jumper #3
- ACB system – with jumper #3 in place

2.12 OPTIONAL COMMUNICATION INTERFACE

- RS-232C PONI - for single point computer communications
- INCOM®/PONI - for local network communications

2.13 CHASSIS DIMENSIONS AND WEIGHT

Height 7" (177.8mm), 4 Rack Units (**See Figure 2-8**)
Width 19" (482.6mm)
Depth 14" (356mm) including terminal blocks
Weight 35 lb. (16Kg net)

2.14 ENVIRONMENTAL DATA

Ambient Temperature Range

- For Operation -20°C to +60°C
- For Storage -40°C to +80°C

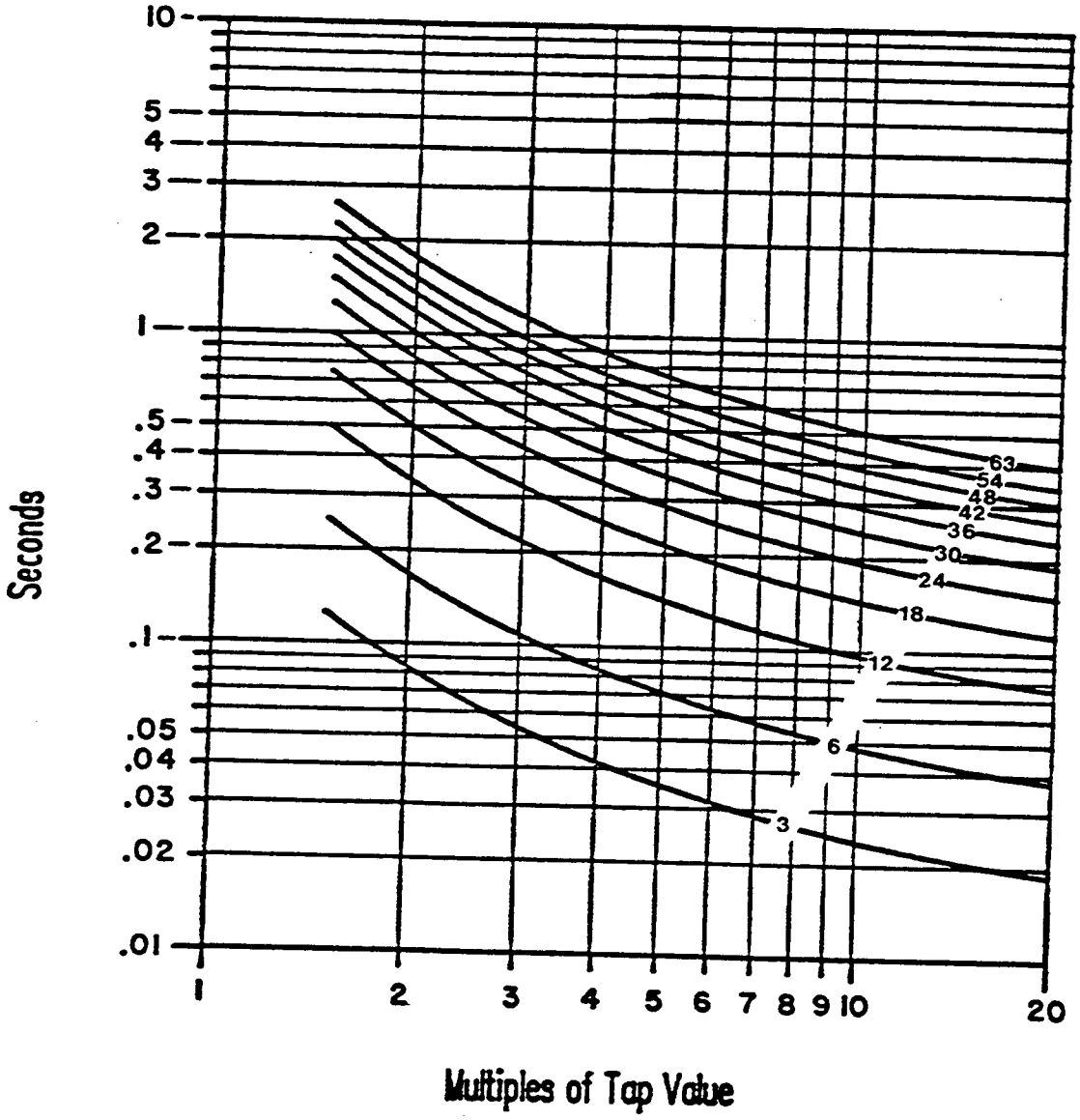
Dielectric Test Voltage 2.8 kV, dc, 1 minute (ANSI C37.90.0, IEC 255-5)

Impulse Withstand Level 5 kV peak, 1.2/50 μsec, 0.5 joule (IEC 255-5)

Fast Transient Surge Withstand Capability 4 kV, 5/50 nsec (IEC 801-4); 5kV 10/150 nsec (ANSI C37.90.1)

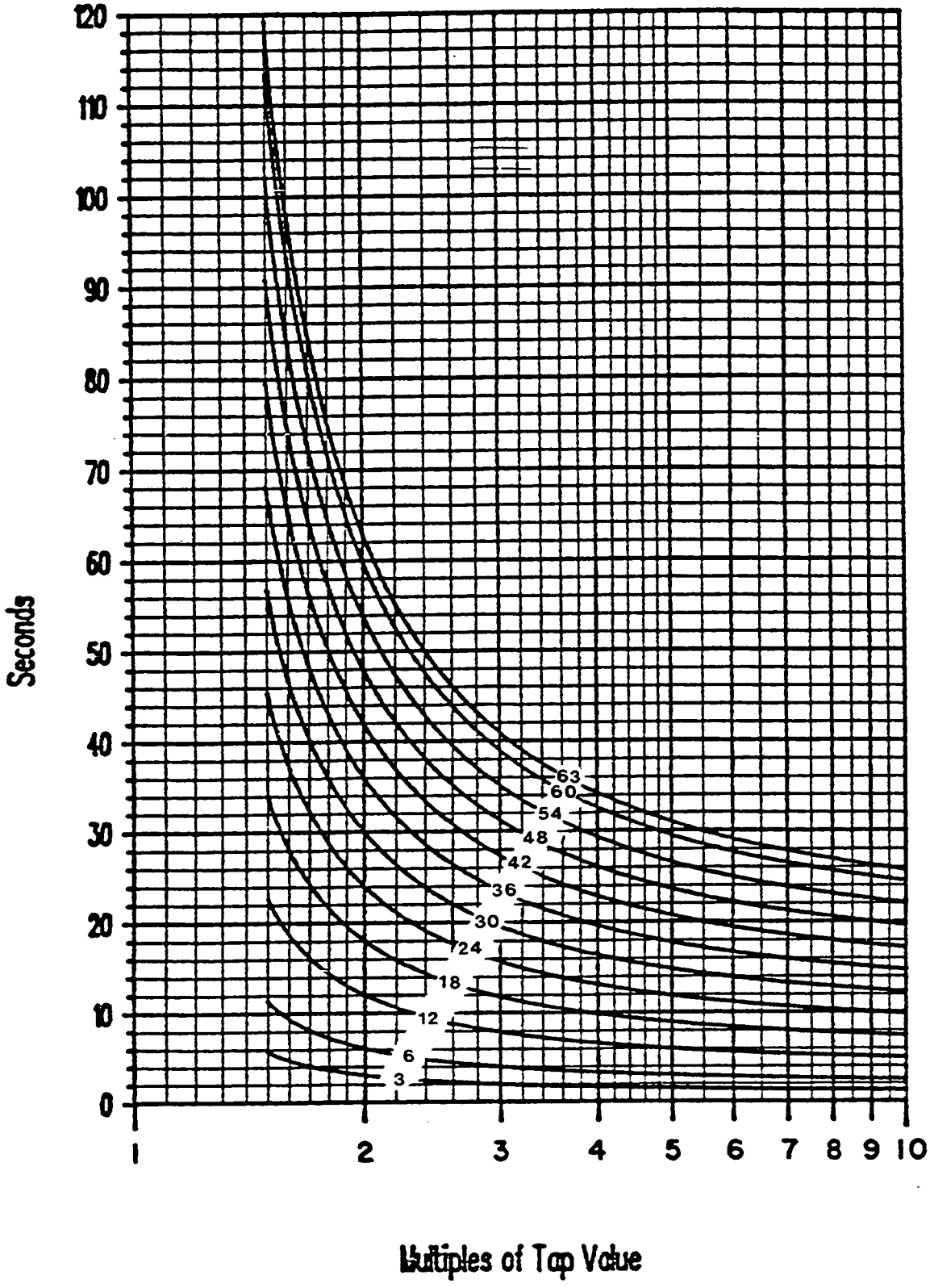
Oscillatory Surge Withstand Capability 2.5 kV, 1 MHz (ANSI C37.90.1, IEC 255-6)

EMI Volts/Meter Withstand 25 MHz-1GHz, 10V/m Withstand (Proposed ANSI C37.90.2).



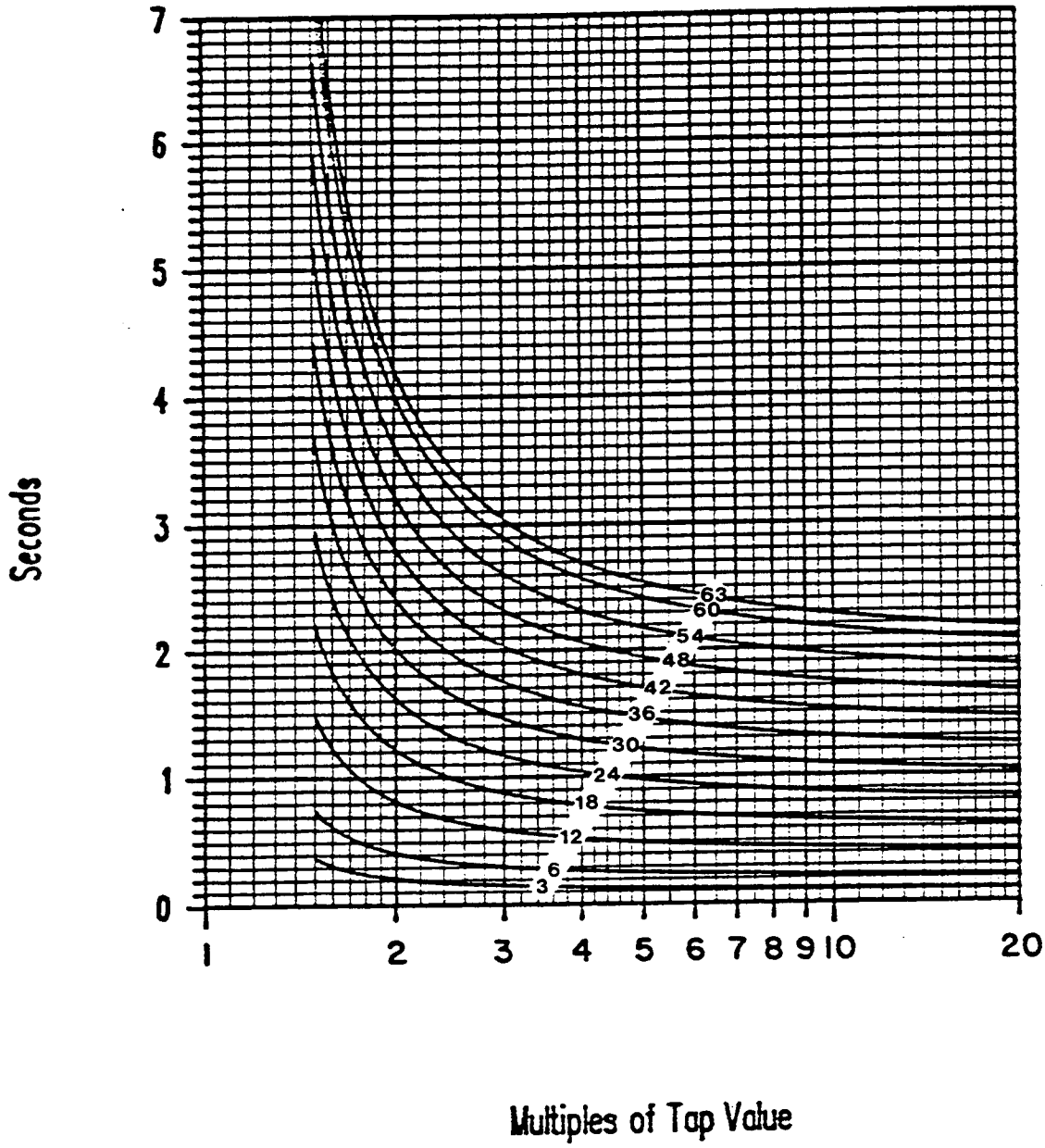
Sub 2
619596

Figure 2-1 CO-2 Curve Characteristics



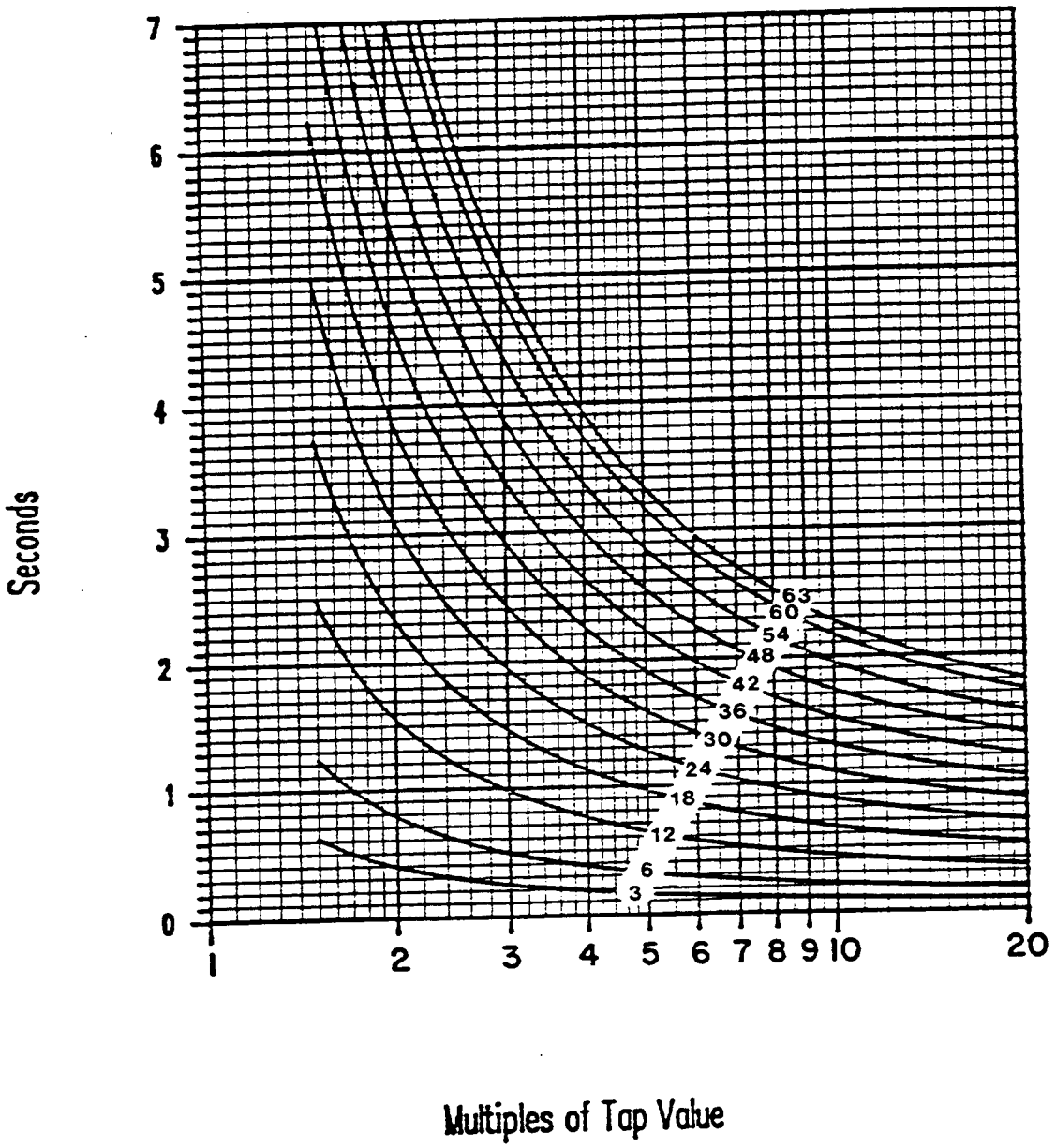
Sub 2
619597

Figure 2-2 CO-5 Curve Characteristics



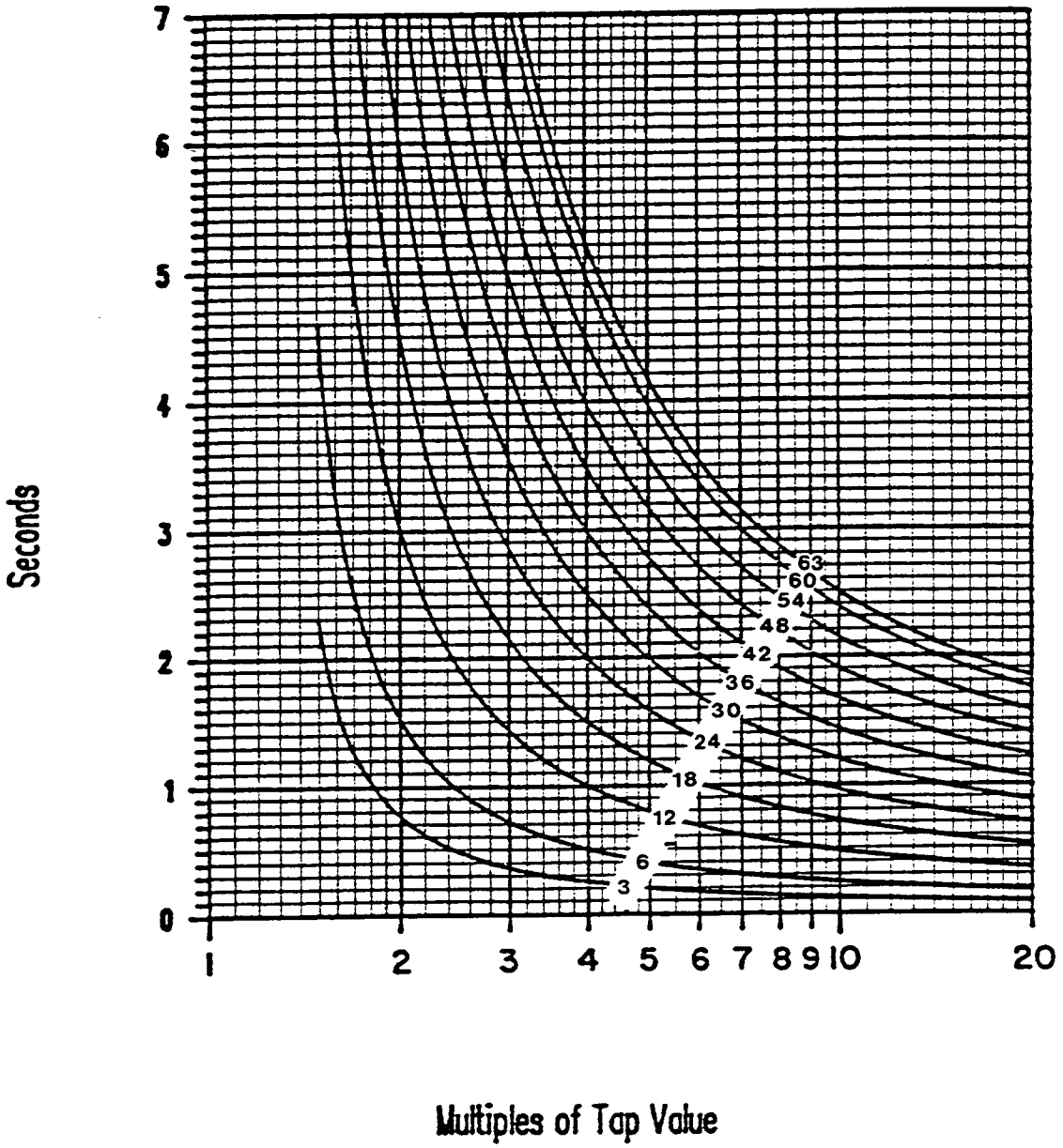
Sub 2
619598

Figure 2-3 CO-6 Curve Characteristics



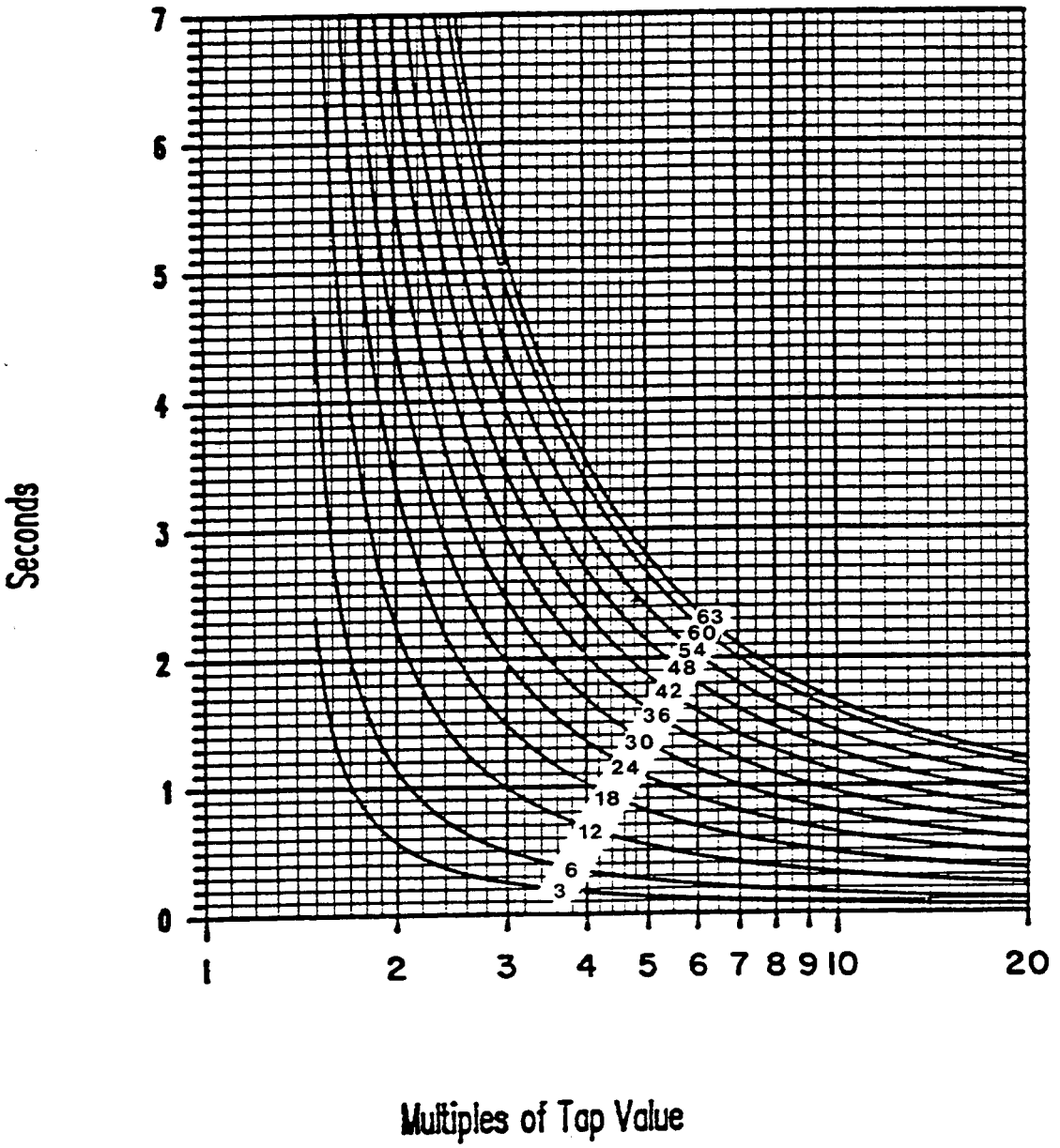
Sub 2
619599

Figure 2-4 CO-7 Curve Characteristics



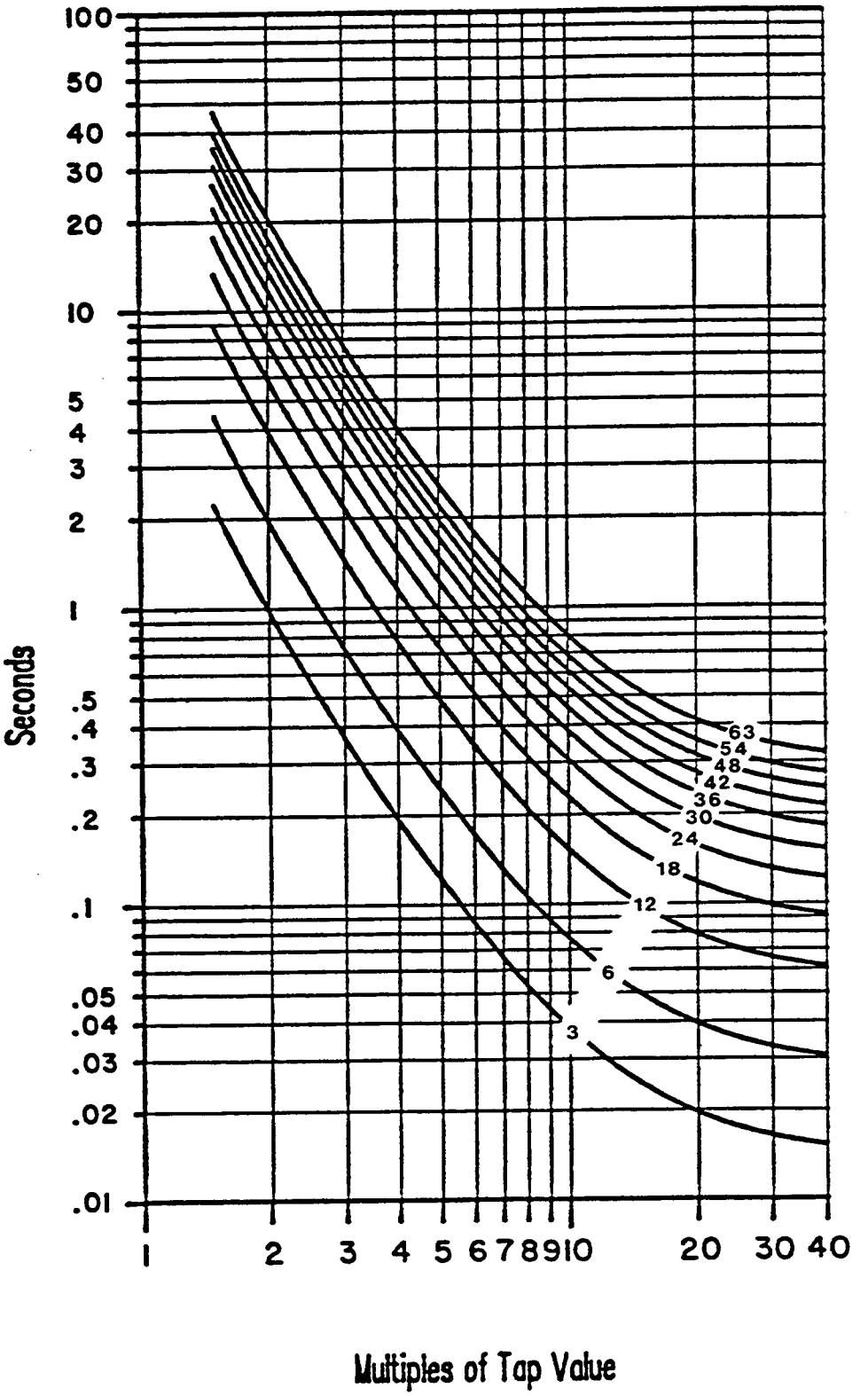
Sub 2
619600

Figure 2-5 CO-8 Curve Characteristics



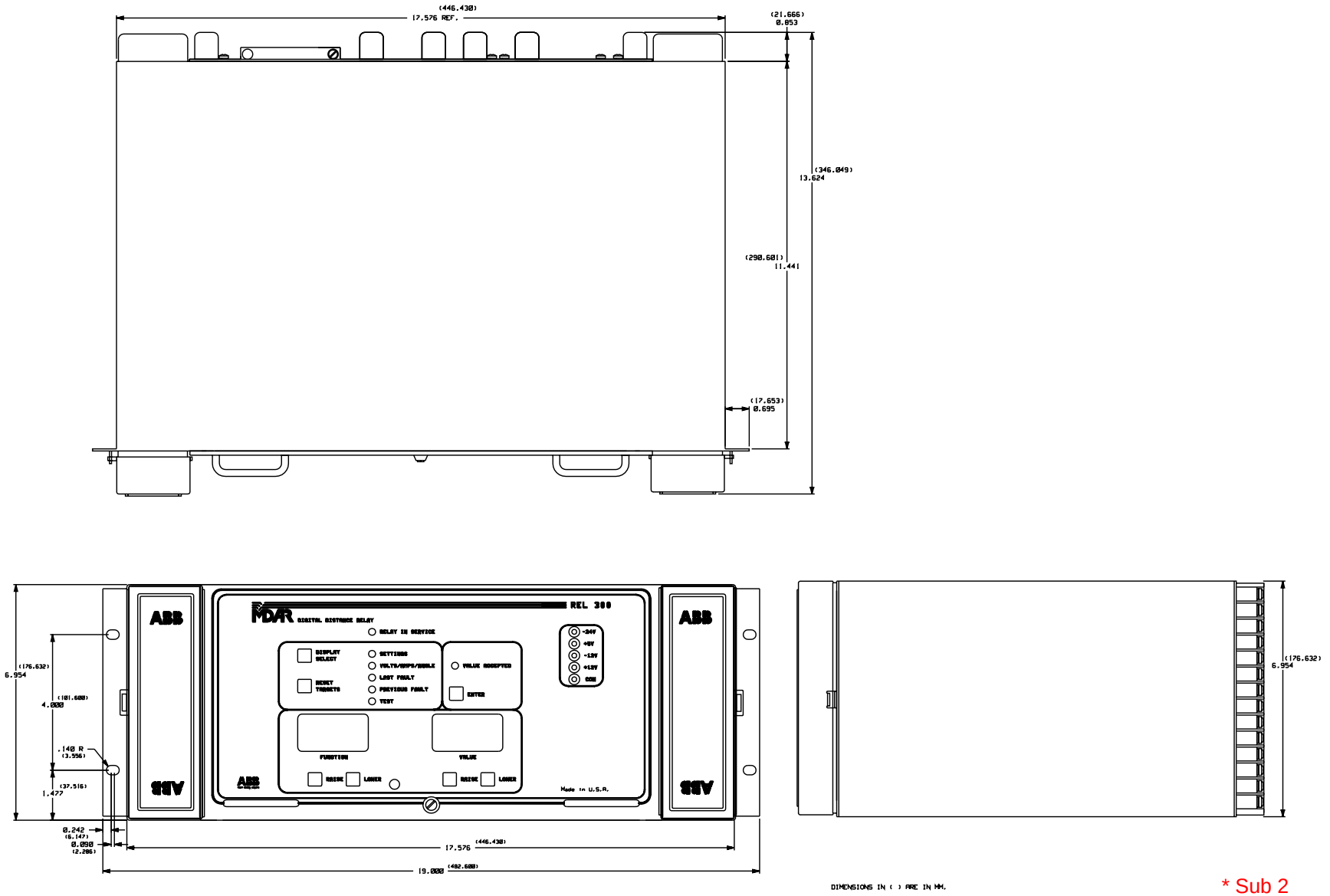
Sub 2
619601

Figure 2-6 CO-9 Curve Characteristics



Sub 2
619602

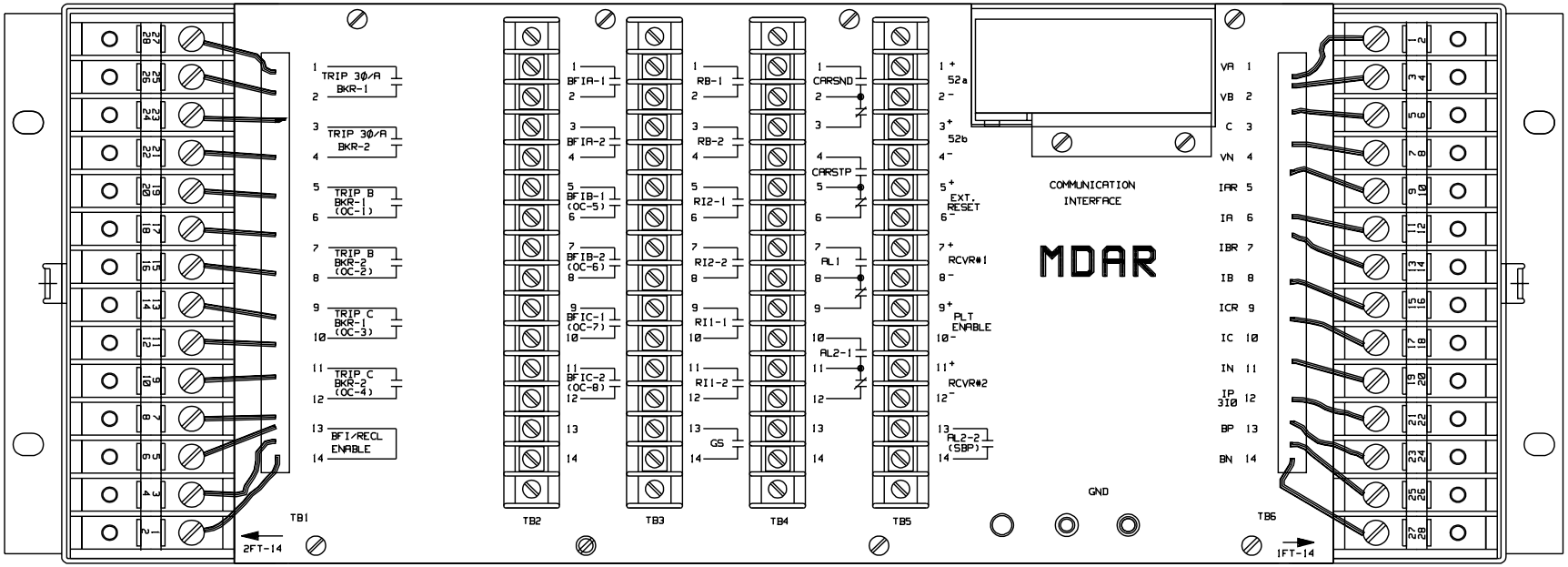
Figure 2-7 CO-11 Curve Characteristics



* Sub 2
2403F38

Figure 2-8 MDAR Outline Drawing

* Denotes Change



NOTE: REFER TO SYSTEM DRAWING FOR THE EXTERNAL WIRING.

Figure 2-9. MDAR Backplane (Rear View)

* Sub 9
2420F01

* Denotes Change

Section 3. APPLICATIONS AND ORDERING INFORMATION

⚠ WARNING

Before energizing the relay, check jumper #3 on the Microprocessor module for phase sequence rotation ABC or ACB. Remove jumper #3 for system ABC rotation. Refer to Section 1.8 for ACB system.

3. 1. NON-PILOT SYSTEM

The MDAR non-pilot relay system detects faults in three zones of distance, phase and ground. Zones-1 and 2 are forward set; Zone-3 can be set to forward or reverse. There is also a separate optional pilot zone (**see Section 3.5**). The fault locator can be set to indicate fault distance in miles or kilometers.

The R-X Diagram **(shown in Figure 3-1)** describes the characteristics available with MDAR. Zone-1 phase and ground settings are chosen to provide substantial coverage of the protected line without overreaching the next bus. A setting of 80% of the line impedance is typical. Faults occurring within the reach of the Zone-1 measurement cause direct tripping without regard to any action occurring at the remote terminal. Zone-2 settings are chosen to assure that faults occurring on the next bus are recognized. Settings are chosen (independent of the Zone-1 settings), generally to be 120 to 150% of the line impedance. Any fault occurring on the protected line will be recognized by this Zone-2 measurement (within the fault resistance and current limitations of the relaying system). Zone-2 tripping occurs with time delay (T2) or, where equipped with pilot provisions, at high speed, subject to the constraints imposed by the pilot channel for the particular pilot system selected. The Zone-3 measurement is directional, and may be chosen to respond to forward or reverse faults. The reverse sensing option is chosen for the blocking system where the reverse fault carrier start function is required. It is also used in conjunction with the T3 trip function, chosen to coordinate with adjacent terminal Zone-2 timing. The forward sensing option produces time delayed backup to other devices sensing forward faults. Blinder measurements (B1, B2, B3, B4) are available for out-of-step sensing. The inner blinder (as a standard function) also restricts the trip zone of each of the 3-phase fault measuring units.

3. 2. LINE MEASUREMENT TECHNIQUES

Line measurement techniques applied to each zone include:

- Single-Phase-To-Ground fault detection
- 3-Phase fault detection
- Phase-to-Phase fault detection
- Phase-to-Phase-to-Ground fault detection

NOTE: IOM is used to supervise all ground units and IM is used to supervise all phase units, including Zone -1,2,3 and pilot for tripping.

3.2.1 Single-Phase-to-Ground

Single-phase-to-ground fault detection (**see Figure 3-2**) is accomplished by 3 quadrature polarized phase units (ϕA, ϕB, ϕC). Equations 1 and 2 (below) are for operating and reference quantity, respectively. The unit will produce output when the operating quantity leads the reference quantity.

$$V_{XG} - [I_X + k_0 I_0]Z_{CG} \qquad (1)$$

$$k_0 = \frac{Z_{0L} - Z_{1L}}{Z_{1L}} = ZR\angle(GANG - PANG) - 1$$

$$I_0 = \frac{1}{3}(I_A + I_B + I_C)$$

Vector (V_Q) (2)

where $V_{XG} = V_{AG}$, V_{BG}, or V_{CG}

I_X = I_A, I_B or I_C

Z_{1L}, Z_{0L} = positive and zero sequence line impedance in relay ohms.

Z_{CG} = Zone reach setting in secondary ohms of Z_{1L} for ϕGF fault

V_Q = quadrature phase voltages, i.e., V_{CB}, V_{AC} and V_{BA} for ϕA, ϕB and ϕC units, respectively.

3.2.2 Three-Phase

Three-phase fault detection (**see Figure 3-3**) is accomplished by the logic operation of one of the three

ground units, plus the 3ϕF output signal from the faulted phase selector unit.

However, for a 3-phase fault condition, the computation of the distance units will be:

$V_{XG} - I_X Z_{CP}$ (3)

and (V_Q) (4)

where V_{XG} = V_{AG}, V_{BG}, or V_{CG}

I_X = I_A, I_B or I_C

Z_{CP} = Zone reach setting (PLTP, Z1P Z2P, and Z3P) in secondary ohms of Z_{1L} for multi-phase faults.

V_Q = Quadrature phase voltages, i.e., V_{CB}, V_{AC} and V_{BA} for ϕA, ϕB and ϕ C units, respectively.

If the MDAR detects that all three voltages are less than 1 volt, the pre-fault voltages (memory action) are used as reference for Zone-1 tripping. For Zone-2 and Zone-3, the memory action is in effect if all three voltages are less than 7 volts.

3.2.3 Phase-to-Phase

The phase-to-phase unit (**see Figure 3-4**) responds to all phase-to-phase faults, phase-to-phase-to-ground faults, and some single-phase-to-ground faults. Equations (5 and 6) are for operating and reference quantity, respectively. They will produce output when the operating quantity leads the reference quantity.

$(V_{AB} - I_{AB} Z_{CP})$ (5)

$(V_{CB} - I_{CB} Z_{CP})$ (6)

3.3 MEASUREMENT ZONES

MDAR performs line measurement within 3 zones of the transmission line (Zone-1, Zone-2, Zone-3), and one optional pilot zone. When the MDAR functional display “STYP” is set at “3ZNP”, it will perform the 3-zone non-pilot function.

When the MDAR trips, the trip contacts will be sealed-in as long as the trip coil current flow exists. The trip contacts can be delayed dropout (by 50 ms) after the trip current is removed, providing a jumper (JMP4) on the Microprocessor module is connected.

3.3.1 Zone-1 Trip

For Zone-1 phase faults, the Z1P unit will identify the fault and operate. The 3ϕ fault logic is supervised by the load restriction logic via AND131C and AND 131 (**Figure 3-18a**) and is also supervised by the selectable OSB, **as shown in Figure 3-5**. Outputs of Z1P and IM satisfy AND-2 and provides a high-speed trip (HST) signal from OR-2 to operate the trip output telephone relay. The trip circuit is monitored by a seal-in reed relay (S), which is in-series with each trip contact in the tripping circuits. The S relay will pick up if the trip current is higher than 0.5 Amp. The operation of the “S” contact will turn-on the breaker trip indicators (with memory), and feeds back to OR-4 to hold the trip relay in operation until the breaker trips and 52a contact opens (not shown in **Figure 3-5**). The TRSL signal plus the output signal from AND-2 turns on the Zone-1 phase trip indicator (Z1P). The breaker trip and Zone-1 phase trip indicators are memorized. They can be reset by external RESET voltage or through remote communication. By pushing the RESET pushbutton, the flashing LED will be reset, but the fault information will still remain in memory.

NOTE: The operating time of the Trip relay is 2 ms and the BFI relay is between 10 and 15 ms. The difference of the pickup times should be compensated in the breaker failure scheme.

The Z1P 3ϕ trip logic AND-131 is supervised by both the conventional OSB and the subsequent OSB logic when the OSB is set to “YES”, for more security on some special power system applications. ZIP logic AND-2 is also supervised by the FDOP (Forward Directional Overcurrent Phase unit) when the OSB is set to “YES” for more security on some special power system applications.

Similar operations exist for Zone-1 single-phase-to-ground faults. The Z1G unit sees the fault and operates; the IOM and FDOG units also operate, satisfying AND-3. Tripping occurs via OR-2 with Zone-1 ground trip indication Z1G. Logic AND-3 is also supervised by the signal of RDOG (reverse directional overcurrent ground) for security purposes.

The Z1G unit is also supervised by the signal of unequal-pole-closing and RDOG.

A two-out-of-three “leading phase blocking” logic is included for solving the overreach problem of the

single-phase ground distance units, which may respond to a ϕϕG fault.

The high-speed trip (HST) signal also is connected to the reclosing initiation logic.

Either or both Zone-1 phase and Zone-1 ground function(s) can be disabled by setting the Z1P and/or Z1G to the “OUT” position. Zone-1 trip can be delayed by setting T1 = YES. The delay time is 2 cycles for a non-pilot 3PT backup, with another system operating in SPT mode.

3.3.2 Zone-2 Trip

For Zone-2 phase faults, the Z2P unit will see the faults plus the output of IMoperate the Zone-2 phase timer (T2P). AND-4 output plus the T2P timer output satisfy AND-18, **as shown in Figure 3-6**. The AND-18 output provides time delay trip signal TDT via OR-3. Signal TDT picks up OR-4 (**Figure 3-5**) and operates the trip relay. The tripping and targeting are similar as described in Zone-1 trip except for Zone-2 phase time delay trip indicator (Z2P).

Similar operation occurs for Zone-2 single-phase-to-ground faults. The Z2G unit sees the fault and operates. This, plus the operation of the IOM, FDOG and T2G satisfy AND-19, and provide the TDT signal via OR-3 with Zone-2 ground time delay trip indicator (Z2G).

The single-phase ground distance units may respond to a ϕϕG fault. The output of the Z2G unit plus the operation of the ϕϕ selection will trip the Z2P via OR-157, T2P and AND-18. Leading phase blocking is unnecessary for an overreach Zone device.

The TDT signal can be connected to the reclosing block logic. The settings for Zone-2 timers (phase and ground units) are independent, as follows:

- T2P (Zone-2 phase)
- T2G (Zone-2 ground)

The range of the timers is as follows:

- T2P and T2G (0.1 to 2.99 seconds or Block)

Either or both Zone-2 phase and Zone-2 ground function(s) can be disabled by setting Z2P and/or Z2G to the BLK position.

3.3.3 Zone-3 Trip

For Zone-3 phase faults, the Z3P (forward or reverse looking, depending on the Z3FR setting) unit will identify the faults, plus the IMIm output will operate the Zone-3 phase timer T3P. AND-6 output plus the T3P timer output satisfy AND-20 (**as shown in Figure 3-7**). The AND-20 output provides time delay trip signal (TDT) via OR-3. Signal TDT picks up OR-4 (**Figure 3-5**) and operates the trip relay. The tripping and targeting are similar to Zone-1 trip, except for the Zone-3 phase time delay trip indicator (Z3P).

For Zone-3 single-phase-to-ground faults, Z3G identifies the fault and operates. This, plus the operation of the IOM, satisfies AND-7; the TDT signal then trips via OR-3 with Zone-3 ground time delay trip indicator Z3G. The TDT signal can be connected to the reclosing block logic. For security, the Z3G unit is also supervised by the signal of FDOG when it is set for forward looking (or by the signal of RDOG when it is set for reverse looking) via logic OR-171B, AND-171C or AND 171D (**as shown in Figure 3-7**).

A similar operation for ϕϕG faults (shown in Zone-2), is applied to Zone-3, through OR-170, T3P and AND-20 gates.

The settings for Zone-3 timers (phase and ground units) are independent, as follows:

- T3P (Zone-3 phase)
- T3G (Zone-3 ground)

The range of the timers is as follows:

- T3P and T3G (0.1 to 9.99 seconds or Block)

Either or both Zone-3 phase and Zone-3 ground function(s) can be disabled by setting Z3P and/or Z3G to the BLK position.

3.3.4 Zone-1 Extension

This scheme provides a higher speed operation on end zone faults without the application of pilot channel.

If the MDAR functional display “STYP” is set on Z1E position, the Z1P/Z1G unit will provide two outputs: one is overreach which is set at 1.25 x Z1 reach by the microprocessor, and one is the normal Z1 reach. A single shot instantaneous reclosing device should be used when applying this scheme. The targets Z1P/Z1G will indicate either Z1 trip and/or Z1E trip

operations. The other functions (e.g., Z2T, Z3T, ac trouble monitoring, overcurrent supervision, ITP, ITG, CIF, unequal-pole closing load pickup control, load-loss acceleration trip, etc.) would remain the same as in the basic scheme (3ZNP).

For a remote internal fault (**refer to Figure 3-8**), either Z1P or Z1G will see the fault since they are set to overreach. High speed trip will be performed via the normal Z1T path (**Figure 3-5**), i.e., AND-2 (or AND-3), OR-2. HST signal operates the instantaneous reclosing scheme. The breaker recloses and stays closed if the fault is automatically cleared.

Target Z1P and/or Z1G will be displayed. Once the breaker trip circuit carries current, it operates the logic OR-5 (not shown), produces output signal TRSL, and satisfies logic AND-26 for 5000 ms (**Figure 3-8**). The output signal of AND-26 will trigger the Z1P/Z1G reach circuit, constricting their reaches back to the normal Zone-1 for 5000 ms. During the reach constricting periods, if the breaker is reclosed on a Zone-1 permanent fault, it will retrip again. If the breaker is reclosed on an end-zone permanent fault, the normal Z2T will take place.

For a remote external fault, either Z1P or Z1G will see the fault since they are set to overreach. High speed trip will be performed. HST signal operates the instantaneous reclosing scheme. The breaker recloses and stays closed if the fault has been isolated by the adjacent line breaker. However, if the adjacent line breaker fails to trip, the normal remote back up will take place.

NOTE: The reaches of Z1E are based on the Zone-1 settings multiplied by a factor of 1.25 (e.g., 1.25 x Z1P and 1.25 x Z1G).

3.4 MDAR NON-PILOT FEATURES

The following features are standard with the Non-Pilot MDAR

3.4.1 3-Zone Distance Phase and Ground Relay with Reversible Zone-3 Phase and Ground

There are four impedance units per zone: one phase-to-phase unit and three phase-to-ground units. Zone-3 can be set to forward or reverse for carrier keying or back-up tripping. For a pilot system, Z3FR has to be set to reverse (REV) for correct application.

3.4.2 Directional or Non-Directional Inverse Time Overcurrent Ground Backup Unit

The overcurrent ground backup (GB) unit is to supplement the distance ground protection on high resistance ground faults. It provides an inverse time characteristic which is similar to the conventional CO characteristics (**see Figure 2-1 thru 2-7)**. The time curves can be selected by the GBCV Setting. The time dial is set by the “GTC” value. The unit can be selected as directional by using the “GDIR” (YES) setting and the pickup value by GBPU. The directional GB function uses the torque control approach, as indicated in **Figure 3-9**. The GB function can be disabled by setting the GBCV to the OUT position.

The directional unit is determined by the setting of “DIRU” which can be set to zero sequence voltage (ZSEQ), dual (DUAL, zero sequence voltage and/or zero sequence current) or negative sequence (NSEQ, negative sequence voltage and negative sequence current) for polarization (**see 3.4.11, Selectable Ground Directional Unit, ZSEQ / NSEQ / DUAL**).

3.4.3 Loss of Potential Supervision (LOP)

The ac voltage monitoring circuit is called loss-of-potential circuit. In order to prevent undesirable tripping due to the distance unit(s) pickup on loss-of-potential, the following logic is used:

- (V_{AN} or V_{BN} or V_{CN} <7Vac) or (3Vo>7Vac) and not ΔI or not ($3I_O$>IOS)

This means that the LOPB will be set if any one of the voltages is below 7Vac (without ΔI), or if the system detects 3Vo without 3Io (or $3I_O$ > IOS) **as shown in Figure 3-10**. The (loss-of-potential condition satisfies AND-1; output signal of AND-1 starts the 8/0 and 0/500 ms timers. The timer output will satisfy AND-1C if there is no output from AND-1B. Output signal of AND-1C will block all the distance unit (Z) tripping paths via AND-2, AND-3, AND-4, AND-5, AND-6, AND-172 (also blocks AND-191 and AND-187 for Pilot Systems), if LOPB is set at YES. Although all distance units are blocked for tripping, the ground backup (GB) and high-set overcurrent units (ITP and ITG) are operative and converted to non-directional automatically. The LOPB blocking function can be disabled by setting the LOPB functional display at NO position. The output of the LOP timer will de-energize the alarm 1 (AL1) relay and cause the failure alarm.

When applying the LOPB to YES, it is the intent to block all distance units from tripping, should LOP condition exist. However, under a special system condition (**refer to Figure 3-11**), both circuits are energized without load current; with no source at terminal B, fault at F where F is near terminal A, Zone-2 relay at terminal B will be blocked by LOP, and may fail to trip. This is because the relay at B sees no current, and a low voltage condition exists before circuit breaker A opens. Another special system condition involves two parallel lines with two symmetrical sources at both ends. For an evolving flashover fault, at a point equidistant from both terminals, the conventional LOPB logic will block trip, because the first external fault generates "3V0 and not $3I_0$"on the protected line. Logic AND-1A, 1B, -1C, and -1E 150/0, 3500/200 ms timers circuit (in **Figure 3-10**) are for solving these problems. This logic unblocks the LOPB circuit and provides a 3500 ms trip window for the distance units to trip if the fault current is detected within 150 ms after LOP has been set up. This logic has no effect on the conditions:

- if ΔI signal occurs ahead of LOP, or
- if LOP and ΔI signals occur simultaneously

NOTE: The LOPB setting detects a blown fuse condition.

The distance units are designed to be blocked under the loss-of-potential condition, but the high set (ITP and ITG) and ground backup (GB) are functional and converted to non-directional automatically (see also 3.4.6).

3.4.4 Loss of Current Monitoring (LOI)

The ac current monitoring circuit uses IOM (and not Vo) as criterion, **as shown in Figure 3-12**. Under ct short circuit or open circuit condition, IOM (and not Vo) satisfies AND-23; the output signal of AND-23 starts the 500/500 ms timer. The timer output turns "ON" the non-memory LOI indicator, which is shown in the Metering mode, and drops out the AL1 relay (Failure Alarm). If the LOI condition exists and LOIB is set at YES, the trip will be blocked after the 500 ms timer times out.

3.4.5 Overcurrent Supervision

For MDAR, **as shown in Figure 3-13**, the distance units do not require overcurrent supervision; because the relay normally operates in a background mode, they will not start the Zone-1 and pilot impedance computation until a phase current or a phase voltage disturbance is detected. This approach can minimize the load problem when setting the phase overcurrent units. However, in order to meet the traditional practice, a medium set phase overcurrent unit IM (IAM or IBM or ICM) has been added to MDAR version 2.10 to supervise Z1P/Z2P/Z3P/PLTP trip functions, **as shown in Figure 3-13**. (Note, older versions do not have this unit). This unit should not be set to limit the Zone-3 reach, and traditionally should be set above the load current.

For coordination purposes the ground trip units (Z1G, Z2G, Z3G, PLTG, and FDOG) are supervised by the medium set ground overcurrent unit (IOM). The IOS setting and RDOG are used for carrier send in a Pilot Blocking system.

3.4.6 Instantaneous Forward Directional Overcurrent Trip/Highset Trip Logic

The instantaneous overcurrent units (IAH, IBH, ICH and IOH) are normally set forward directional and high to detect those faults which occur in the Zone-1 area, therefore, their tripping will occur via OR-2 for HST, **as shown in Figure 3-14**. These high set trip functions can be disabled by setting the ITP (phase) and/or ITG (ground) to the OUT position. The directional unit (ITP and ITG) will be automatically converted to non-directional protection if the LOP condition occurs and the setting of LOPB = YES.

3.4.7 Close-Into-Fault Trip (CIFT) and Stub-Bus Protection (SBP)

There are three low voltage units (LVA, LVB and LVC) in MDAR. Each unit senses the phase voltage condition in the background mode. The unit can be set from 40 to 60 volts, in 1.0 volt steps. For any phase voltage below its preset value, the LV logic will produce a logic "1" output signal. The low voltage units are used in CIFT and weakfeed logic in MDAR.

In order to supplement distance unit operation, when the circuit breaker is closed into a fault and line side potential is used, the Close-Into-Fault Trip (CIFT) circuit operates **as shown in Figure 3-15**. It includes logic AND-22, OR-3 and 100/180 ms and 16/0 ms timers. If any overcurrent unit (IAL, IBL, ICL or IOM) operates OR-11, at the same time as one of the phase voltages (VA, VB,VC) is below the preset level of the LV units. Then logic AND-22 is satisfied and produces a trip signal (for 180 ms) after circuit breaker closes (52b contact opens). Tripping will be via OR-3, with RB and CIF targets.

The stub bus protection feature protects a line terminal with the potential device on the line-side. With the line disconnect switch open, the distance units will lose their reference voltage, and may not function correctly when a fault occurs on the short part of the bus between the ct location and the opened disconnect switch. The logic for stub bus protection is independent of the operation of the circuit breaker(s) and the line voltage condition. Also, it requires the information from the disconnect switch (89b). The stub bus protection logic, **as shown in Figure 3-15**, includes the contact convertor for the 89b switch and AND-22E and OR-22B logic.

The application of "close-into-fault" and "stub-bus protection" are selected by setting the value field of CIF to CIFT/STUB/BOTH/NO.

3.4.8 Unequal-Pole-Closing Load Pickup Logic

The ground units may pick up on a condition of load pickup with unequal breaker pole closing. The high speed ground units (Z1G, and FDOG) should be supervised under this condition. This can be achieved (**as shown in Figure 3-16**) by inserting a 0/50 ms timer (controlled by the 52b signal) to supervise the Z1G trip AND-3 (**Figure 3-5**) and FDOG/IOM trip AND-188 (**Figure 3-21 and 3-26**). It should be noted that the 50 ms time delay will have no effect on a normal fault clearing.

Pilot distance ground PLTG unit is not required to have this supervision, because its tripping is supervised by the pilot logic.

On internal ground faults, if the mechanical actuator of the circuit breaker operates but the arc does not extinguish (e.g., due to low gas pressure), the closing action of the 52b contact, connected to MDAR, will reset the Z1G trip path AND-3, and ultimately, the BFI contact. This may introduce interruption to the BF scheme if BFI logic does not provide seal-in circuit. The AND-3C logic in **Figure 3-16** will solve this problem.

3.4.9 Selectable Loss-of-Load Accelerated Trip Logic (LLT)

NOTE: The LLT function need not be set for normal operation of the relay. While it can provide faster tripping for end-zone faults, it may not be usable in all situations. It should be applied with caution, based on thorough knowledge of the system characteristics where the relay is applied. It is definitely not applicable where maximum tapped load may exceed minimum through-load in the protected line.

The load-loss speedup Zone-2 trip logic senses remote 3-pole clearing on all faults except 3ϕF to complement or substitute for the action of the pilot channel, to speed up trip at the slow terminal. Logic includes AND-24, AND-25, OR-13, 0/32, and 10/0 ms timers (**as shown in Figure 3-17**). Under normal system conditions, 3-phase load currents are balanced, the low set overcurrent units (IAL, IBL, ICL satisfy both AND-24 and OR-13). On remote internal faults, Z2P or Z2G picks-up and satisfies the third input to AND-25 via OR-6. However, the signal from AND-24 is negated to AND-25, therefore, AND-25 should have no output until the remote end 3-pole trips. At this time, the local end current will lose one or two phases, depending on the type of fault (except for the 3-phase fault). The AND-24 output signal changes from "1" to "0" and satisfies AND-25. After 10 ms, this output by-passes the T2 timer, and provides speedup Zone-2 trip. The (10/0 ms) time delay is for coordination on external faults with unequal pole clearing. The 0/32 ms timer is needed for security on external faults without load current condition. Target LLT will turn on after a LLT trip. The LLT function is selected by setting "YES, FDOG, NO", where YES = LLT with Z2 supervision; FDOG = LLT with both Z2 and (FDOG/I_{OM}) supervision; the NO = LLT function is not used.

LLT is not recommended for three-terminal line due to difficulty in determining proper settings (IL) and complicated infeed from the third terminal.

3.4.10 Current or Voltage Change Fault Detector (ΔI, ΔV) and GS

The MDAR relay normally operates in the Background mode, where it experiences phase current or voltage disturbances. During background mode, the four input currents (I_A, I_B, I_C and I_P) and the three voltages (V_A, V_B, V_C) are sampled at a rate of 8 per cycle to test a line fault. When a phase disturbance (ΔI or ΔV) is detected, the relay enters a fault mode for several cycles or longer, to perform phase and ground unit distance computation for each goal. The criteria for determining a disturbance in the MDAR design are as follows:

1) Each phase ΔI: if $[I_{Kn} - I_{(K-1)n}] > 1.0$ amp.
   And $[I_{Kn} - I_{(K-1)n}] / I_{(K-1)n} \times 100\% > 12.5\%$

2) Each phase ΔV: if $[V_{Kn} - V_{(K-1)n}] > 7.0$ volts and $[V_{Kn} - V_{(K-1)n}] / V_{(K-1)n} \times 100\% > 12.5\%$

3) ΔI_0: if $[(3I_0)_{Kn} - (3I_0)_{(K-1)n}] > 0.5$ amp.
Where n = 1, 2, 3, 4, 5, 6, 7, 8 and
K = number of cycles

For every voltage or current disturbance, the General Start (GS) relay will pick up for 3 cycles for starting external (fault) recorder.

3.4.11 Selectable Ground Directional Unit (ZSEQ/NSEQ/DUAL)

The ground directional unit (DIRU) contains three selections (ZSEQ, NSEQ and DUAL), which determine the operation of the forward directional overcurrent ground (FDOG) and reversed directional (RDOG). If the ZSEQ is selected, both FDOG and RDOG units will be operated as a zero-sequence voltage polarizing directional element. Forward direction is identified by the angle, if $3I_0$ leads $3V_0$, between 30° and 210°. The sensitivity of this element is $3I_0 > 0.5$A and $3V_0 > 1.0$ Vac. If NSEQ is selected, both FDOG and RDOG will be operated by negative sequence quantities. The maximum sensitivity for the forward directional unit is when I_2 leads V_2 by 98°, with $V_2 \geq 1.0$ Vac and $3I_2 \geq 0.5$A.

If DUAL is selected, the FDOG and RDOG will be determined by either zero-sequence voltage polarizing element, as the setting of ZSEQ or current polarizing directional element (I_P), which is connected to 1FT-14, switch #12 and switch #11 is from power transformer neutral (ct). The maximum torque angle between $3I_0$ and I_P equals zero degrees, i.e., the forward direction is identified when $3I_0$ leads I_P by 0° to 90° or lags by 0° to 90°. The sensitivity of this element is $3I_0 > 0.5$ and $I_P > 0.5$ Amps.

3.4.12 Instantaneous Forward Directional Overcurrent Unit (FDOG) and Phase Unit (FDOP)

The instantaneous forward directional overcurrent ground function (FDOG) is a directional unit depending on the setting of DIRU as described in the preceding segment (3.4.11). FDOG is supervised by the IOM setting and controls Zone-1, Zone-2 and Zone-3 ground units for security purposes and also for pilot high resistance ground fault trip (FDOG/I_{OM}).

The phase directional unit (FDOP) is based on the angular relationship of a single-phase current and the corresponding phase-to-phase voltage phasors. The forward direction is identified if the current phasor leads the voltage phasor. The pair of current and voltage phasors which are compared are I_A and V_{BA} (FDOPA), I_B and V_{CB} (FDOPB), I_C and V_{AC} (FDOPC).

3.4.13 Instantaneous Reverse Directional Overcurrent Ground Function (RDOG)

Similar to FDOG, the instantaneous reverse directional overcurrent ground function (RDOG) supervises the ground units to prevent false trip.

3.4.14 Programmable Reclosing Initiation and Reclose Block

The MDAR system provides the following contact output for Reclosing Initiation and reclosing block functions (**see Figure 3-19**):

- RI1, used for Reclosing Initiation on single pole trip
- RI2, used for Reclosing Initiation on 3-pole trip
- RB, used for Reclosing Block

The operation of RI1, RI2 and RB contacts is controlled by the setting of the programmable Reclosing Initiation logic (**as shown in Figure 3-19**). The operation of either RI1, RI2, or RB must be confirmed by the signal of TRSL, which is the trip output of MDAR operation.

The External Pilot Enable Switch (**see Figure 4-1**, TB-5 terminals 9 and 10), is used for enabling the pilot system externally. The PLT setting is similar to the external pilot enable switch, except it is set from the front panel (or remotely set via communication chain).

The most popular Reclosing Initiation practice is to have Reclosing Initiation on high speed (pilot, Zone-1 and high set) trip only. Programming can be accomplished by closing the pilot enable switch and setting the PLT and Z1RI to YES (**see Figure 3-19**). AND-84 will produce logic to operate the RI2 relay when receiving signals from TRSL and AND-89 and no signal from RB logic. The program is further controlled by the TTYP setting: TTYP setting OFF: 3PRN provides no output, therefore, will not operate RI2.

TTYP setting 1PR: 3PRN will provide output “1” on single-phase-to-ground fault only and will operate RI2.

TTYP setting 2PR: 3PRN will provide output “1” on single-phase-to-ground fault or 2-phase faults, and will operate RI2.

TTYP setting 3PR: 3PRN will provide output “1” on any type of fault, and will operate RI2.

The Z1RI, Z2RI and Z3RI settings are provided for programming on applications where the Reclosing Initiation on Zone-1, Zone-2 or Zone-3 trip is desired. Logic AND-62a is controlled by the signal of 3PRN, therefore, the setting of 1PR, 2PR and 3PR also affect the Z1RI, Z2RI and Z3RI.

In general, the Reclosing Block (RB) relay will operate on TDT (Time Delay Trip) or OSB (Out-of-Step Block condition). However, it will be disabled by the setting of Z1RI, Z2RI, and Z3RI signal.

The RI1 relay is normally used for the single-pole trip scheme. A Breaker Failure Reclosing Block (BFRB) feature is available for pilot systems if RB is required for breaker failure squelch. **Refer to section 3.21** for the detailed information.

3.4.15 Output Contact Test

A “Push-to-Close” feature is included in order to check all output relay contacts, which include TRIP, BFI, RI1, RI2, RB, AL1, AL2, GS, Carrier Send, Carrier Stop and all programmable contacts (OC1 to OC8).The relay contact check is supplementary to the self-check because the Microprocessor self-check routine cannot detect the output hardware. In order to enable the contact test, jumper (JMP5) on the Microprocessor module must be connected. (**See Appendix H, 1.1.13, Step 35** for detailed procedures.)

3.4.16 Sixteen Fault Data

The MDAR system saves the latest sixteen fault records for all zones. The latest two fault records can be accessed either via the front panel or via the communication port. Fault records 3 thru 16 can only be accessed via the communication port. On the front panel, the “LAST FAULT’ information is of the last fault, the “PREVIOUS FAULT” information is of the previous fault. These displays contain target information. When targets are available, the LAST FAULT LED flashes. It flashes once per second if only the LAST FAULT contains targets. It will flash twice per second if two or more fault records are contained. These records can be deleted by applying a rated voltage to the Ext. Reset Terminals (TB5/5 and TB5/6), or through a remote communication interface. By pressing the Reset pushbutton, the LED will be reset to the Metering mode and the fault information will still be retained.

The activation of fault data storage is controlled by the selection of TRIP/Z2TR/Z2Z3 in the FDAT function, where:

TRIP --- start to store fault data only if trip action occurs.

Z2TR --- start to store fault data if Zone-2 units pick up or any trip action occurs.

Z2Z3 --- start to store fault data if Zone-2 or Zone-3 units pick up or any trip action occurs.

3.4.17 Out-of-Step Block (OSB) Logic

The Out-of-Step Blocking (OSB) logic (power swing block supervision) in MDAR is a double blinder scheme. It contains two blinder units, providing 4 blinder lines. The nature of the logic (shown in **Figure 3-18a**) is that the outer blinder 21BO must operate 50ms or more ahead of the inner blinder 21BI, in order for an OSB condition to be identified. The OSB logic is also supervised by the medium set (IM) phase overcurrent signal (AND-122 on **Figure 3-18a**). The OSB signal is a negated input to the AND-131 (Z1P), AND-147 (Z2P), AND-160 (Z3P), and AND-176 (PLTP) for supervising the 3-phase distance trip. In addition to controlling the OSB logic, the blinder units also may be used to supervise distance relay tripping. Phase distance unit tripping cannot take place unless 21BI operates. This prevents operation of the 3ϕ-unit of the distance relay on load. The OSB signal is also applied to the reclosing logic for initiating RB.

The following quantities are used for the blinder sensing:

Blinder Line	Polarizing	Operating
Left	$-j(V_{XG} + I_X R_C - (PANG - 90°)$	I_X (PANG–90°)
Right	$j(V_{XG} - I_X R_C - (PANG - 90°)$	I_X (PANG–90°)

where VXG = Phase to ground voltage, V_{AG} or V_{BG}

I_X = Phase current in ϕA or ϕB

R_C = Setting of the unit (RT or RU). RT for inner blinder (21BI), RU for outer blinder (21BO).

PANG = The positive sequence line impedance angle.

Operation occurs if the operating voltage leads the polarizing voltage. The characteristics are **as shown in Figure 3-18b**.

Both inner and outer blinders are included in phases A and B for OSB detection on the SPT application. Blinder reaches are determined by the setting of RT and RU, respectively.

2.14.0.1 Security Logic for Subsequent Out-of-Step (OS) Condition

Model power system tests, when using a motor-generator-set, show that the Zone-1 impedance unit may overreach or respond to a reversed fault. This was attributable to motor-generator set instability following delayed clearing on an external fault. In this case, following a delayed clearing of external faults, the relay system action is dependent of the location of the electrical center. The Zone-1 relay will operate and trip if the electrical center is within the Zone-1 reach. The conventional OSB logic can not distinguish this condition because it looks like a fault to the relay.

Logic was added utilizing the inner blinder and Zone-1 sensing sequence, plus a 50 ms timing action (**as shown in Figure 3-18a**), AND-131A, AND-131B, AND-131C and OR-122A, to differentiate between a fault and a subsequent out-of-step condition. A subsequent OS condition is identified if the inner blinder operates 50 ms ahead of the Zone-1 3ϕ unit. This logic will not affect normal Zone-1 trip time, nor will it affect normal out-of-step blocking.

3.4.18 Optional Single-Pole-Trip (SPT) Logic and Outputs Without Programmable Contact Option

The logic for Single-Pole-Trip operation provides the following functions (**see Figure 3-20**):

- Single-pole-trip (SPT) and single-pole reclosing initiate (RI1) on single-phase-to ground faults.
- Three-pole-trip (3PT) with three-pole-reclosing initiate (RI2) on all multi-phase faults.
- Three-pole-trip with or without three-pole reclosing initiate on all faults if the functional display trip-mode selector “TTYP” is not set on the SPR or SR3R position.
- Three-pole-trip and reclosing block (RB) on unsuccessful reclosing.
- Three-pole-trip and reclosing block on “sound phase fault” (SϕF) during single-phasing.
- Three-pole-trip and reclosing block when the single phasing limit timer (62T, 300-5000,in 50 ms steps) is timed out to prevent overheating on generator(s).

When applying SPT, the functional display TTYP settings (OFF/3PR/SPR/SR3R) provide the following operating modes (in **Table 3-3**).

3.4.19 Oscillographic Data

The oscillographic data has 8 samples per cycle, 1 cycle pre-trigger and 7 cycles post-trigger. It includes 16 events and 24 digital intermediate targets (test points). The data can be accessed via the communication port.

The oscillographic data is controlled by the selection of TRIP/Z2TR/Z2Z3/$\Delta V \Delta I$ in the OSC function, where:

TRIP — start data taken only if trip action occurs

Z2TR — start data taken if Zone-2 units pick up or any trip action occurs.

Z2Z3 — start data taken if Zone-2 or Zone-3 units pick up, or any trip action occurs.

$\Delta V \Delta I$ — start data taken if ΔI, ΔV, Zone-2 or Zone-3 units pick up, or any trip action occurs.

NOTE: See 4.9 for $\Delta V \Delta I$ setting.

3.5 PILOT SYSTEM

The MDAR functional display (**see Section 4, Table 4-1, Sheet 1 of 3**) Function Field “STYP” is used for pilot system selection, as follows:

- Non-pilot, 3-zone distance
- Zone-1 extension (non-pilot)
- POTT (Permissive Overreach Transfer Trip/ Simplified Unblocking).....(pilot)
- PUTT (Permissive Underreach Transfer Trip).....(pilot)
- BLK (Blocking).....(pilot)

The following settings are recommended for POTT and BLOCKING systems:

OSC	-	Z2Z3
FDAT	-	TRIP
FDGT	-	longer than 3 cycles
PLTP/PLTG	-	150% overreach the next bus
Z1P/Z1G	-	80% of the protected line
Z3P/Z3G	-	100% of the reversed line
Z3FR	-	REV

3.5.1 Permissive Overreach Transfer Trip (POTT)/Simplified Unblocking

If the functional display “STYP” is set at the POTT position, MDAR will perform either the POTT scheme or the Simplified Unblocking scheme, depending on the applied pilot channel.

The basic operating concepts of a POTT scheme are:

(1) Pilot relays (PLTP/PLTG) are set to overreach the next bus.

(2) Pilot channel is a frequency shift type device; its signal may be through either metallic wire or microwave.

3) Transmitter frequency should be different at each terminal: channel is normally operated on a guard frequency; and the channel frequency will be shifted from guard to trip when the pilot relay(s) are operated; and pilot trip is performed when the pilot relay(s) operate(s) and a pilot trip frequency signal from the remote end is received.

The basic operating concepts of a Simplified Unblocking scheme are the same as the POTT scheme, except for differences in application.

Pilot channel is a frequency-shift type power line carrier. The transmitter frequency must be different at each terminal. It is normally operated on a blocking frequency and will be shifted to an unblocking frequency when the pilot relay(s) operate(s). The carrier receiver should provide logic for which, in the event of loss-of-channel or low SNR ratio, the pilot trip circuit is automatically locked out after a short time delay. Pilot trip is provided, however, if the tripping distance relay(s) operate(s) during this short time period between loss-of-channel and pilot trip lockout. ABB type TCF-10B receiver provides this logic; it provides a 150 ms trip window, then automatic lockout after loss-of-channel. Provision for a second high-speed pilot trip is provided, for the situation when a permanent fault causes a permanent loss-of-channel and the breaker closes onto the fault.

Indication for low signal and loss-of-channel condition will not be provided for this simplified unblocking scheme. (This function would normally be incorporated in the power line carrier equipment.)

The operating concepts of the pilot distance measurement units (PLTP/PLTG) are the same as for the non-pilot zone distance measurement units, and are supervised by the same LOPB, OSB, IM, IOM, FDOP, and FDOG, units, **as shown in Figure 3-21**. The pilot phase and/or pilot ground function(s) can be disabled by setting the PLTP and/or PLTG to the OUT position.

The POTT and Simplified Unblocking schemes include the following kinds of logic:

a. Tripping logic (**Figure 3-22**)

(1) For a forward external fault, the local pilot relay (PLTP and/or PLTG) sees the fault, operates and keys. The output from OR-40 will satisfy the first input to AND-30. Assuming that reverse block (TBM) logic does not operate and pilot enable is set, then three out of four inputs of AND-30 are satisfied, but pilot trip should not occur since the remote transmitter still sends a guard (or blocking) frequency signal.

(2) For an internal fault, the pilot relays at both ends (PLTP and/or PLTG) see the internal fault and operate; in addition, the overcurrent supervision output(s), together with the received trip (or unblocking) frequency signal CR via AND-44 (in **Figure 3-23**), satisfy AND-30 (in **Figure 3-22**). Pilot trip signal PT will be applied to OR-2 (in **Figure 3-5**) from AND-30. High speed pilot trip (HST) would be obtained. Targets of pilot phase trip (PLTP) and/or pilot ground trip (PLTG) will be turned-on after the breaker trips.

b. Carrier Keying Logic (**Figure 3-23**)

(1) Forward Fault Keying

For a forward internal or external fault, the local pilot relay (PLTP and/or PLTG) sees the fault and picks up, operates OR-40, AND-45, OR-18, and AND-35 if pilot enable is set, and functional display “STYP” is set at POTT position. Output signal from AND-35 will operate the reed relay (CARSND), key the local transmitter, shift the transmitting frequency from guard to trip (or from a blocking to an unblocking), to allow the remote pilot relay system to trip.

(2) Echo Keying

Since the POTT and the Simplified Unblocking schemes require the receiving of a permissive signal from the remote end, for pilot trip, provision should be made for covering the condition when the remote breaker is opened.

When the remote breaker is opened, the inputs of AND34B (**Figure 3-23**) will satisfy the NOT FORWARD, NOT REVERSE and 52b=1 conditions. Any carrier RCVR (CR) will produce an output from AND 34B and also a SEND signal from AND 35 via OR-18. This echo keying will be stopped by itself after 150 ms due to the input timer of AND 34B.

(3) Signal Continuation

This logic includes the signal of TRSL, 0/150 ms timer, AND-34A, OR-18, and AND-35. The 0/150 ms signal continuation time is required to keep the local transmitter at the trip frequency (or unblocking) for 150 ms after the local breaker trip signal TRSL is present, in case of sequential trip on the system. This logic will be disabled by the signal via TDT, the 0 / 300 ms timer (AND-34A) on any time delay trip operation. The signal continuation logic will not perform if the trip is caused by CIF trip (AND 49A).

c. Carrier Receiving Logic (**Figure 3-23**)

This logic includes OR-15 (not shown) and AND-44. Output “trip” (or unblocking) frequency signal from the carrier receiver operates the logic OR-15 and will produce a carrier trip (CR) signal from AND-44.

d. Channel Indicators (**Figure 3-23**)

The memorized SEND indicator will be displayed after the breaker trips and the frequency shifts to trip or unblocking by the transmitter during the fault. The memorized RCVR indicator will be displayed after the breaker trips and a carrier trip signal is received from the receiver.

e. TBM, Transient Block and Unblock Logic

For a loop system or a paralleled line application, power reversal may introduce problems to the pilot relay system especially when a 3-terminal line is involved, since the distance units may have to be set greater than 150% of ZL in order to accommodate the infeed effect from the tapped terminal. They may see the external fault on the parallel line when the third source is out of service. The transient block and unblock logic (TBM) is used to solve this problem.

There are some other typical cases of the protected line being tripped by a ground directional relay upon clearing of a fault in the adjacent (but not parallel) line. When the adjacent line breaker trips, it interrupts the current in the faulted phase as well as the load current in the unfaulted phases. Dependent on the direction of this load current, and the contact asymmetry of the breaker, there can be a short pulse of load-derived I_0 with possible “tripping direction” polarity, which provides an electrical forward-torque to the ground directional relay. Therefore, it is desired to increase the security and the transient block timer (0/50) logic will be included automatically in the application if STYP = POTT is set. ***For* POTT *application, the Z3FR setting MUST be set to “REV” and Z3P, Z3G should be set to 100% of the line impedance.***

f. Channel Simulation

The test function selection provides the capability to simulate the “TK” switch function for keying action via OR-18 and AND-35 without the operation of pilot relay units, and to simulate the RS switch function for receiving of a trip or unblocking frequency signal action without the operation from the remote transmitter.

g. Programmable Reclosing Initiation (**Figure 3-19**)

The basic programmable RI application is as described in **Section 3.4.14**. However, on pilot systems, to activate the RI2 on any 3-pole high-speed trip, the external pilot enables switch should be ON, and the PLT and Z1RI should be set to YES. The op-

eration will occur via the logic AND-89, AND-84 and OR-84A (**as shown in Figure 3-19**).

3.5.2 Permissive Underreach Transfer Trip (PUTT)

The basic operating concepts of a PUTT scheme are:

(1) Pilot relays (PLTP/PLTG) are set to overreach. The pilot channel is a frequency-shift type device, and the transmitter frequency should be different at each terminal; its signal may be passed through metallic wire or microwave.

(2) Channel is normally operated with a guard frequency, the channel frequency will be shifted from guard to trip when the Zone-1 reach relay (Z1P/Z1G) operates, and pilot trip is performed when the pilot relay (PLTP and/or PLTG) operates, together with the receiving of a carrier trip signal from the remote end.

PUTT includes the following logic: the functional display (STYP) should be set to PUTT position.

a. Pilot Tripping Logic

The Pilot Tripping Logic for the PUTT scheme is exactly the same as for the POTT scheme (**Figures 3-21, 3-22**).

b. Carrier Keying Logic

(1) Forward fault keying (**Figure 3-24**)

For a forward end zone fault, the PUTT scheme will not key except when the internal fault is within Zone-1. This means that the PUTT scheme keys only on Zone-1 faults. Keying flows via AND-46, OR-18 and AND-35.

NOTE: For open breaker condition, the echo keying will not work due to lack of the "SEND" signal from the remote terminal for an end zone fault. The remote terminal relies on Zone-2 to clear the fault.

(2) Signal continuation (**Figure 3-23**)

Same as for POTT scheme.

The TBM logic is not required because the carrier keying units are set underreach.

c. Programmable Reclosing Initiation (**Figure 3-19**)

Same as for POTT scheme.

d. Carrier Receiving Logic (**Figure 3-23**)

Same as for POTT scheme.

e. Channel Indicators (**Figure 3-23**)

Same as for POTT scheme.

3.5.3 Directional Comparison Blocking Scheme (BLK)

The basic operating concept of a Directional Comparison Blocking system (BLK) are:

(1) Pilot relays (PLTP/PLTG) are set to overreach; the Zone-3 relays (Z3P/Z3G) must be set in the reverse direction to detect the reverse external faults and for carrier start.

(2) Pilot channel is an "ON-OFF" type power line carrier. Transmitter frequency at each terminal can be the same. Channel is normally OFF until the carrier start relay senses the fault and starts the transmitter.

(3) Pilot trip is performed when the pilot relay(s) operate(s) and a carrier blocking signal is not received.

The BLK system, **as shown in Figure 3-25**, includes the following logic (functional display "STYP" should be set at the BLK position):

a. Tripping Logic (**Figure 3-25**)

(1) For a forward internal fault, the local pilot relay (PLTP and/or PLTG) sees the fault; output signal of OR-40 disables and stops the carrier start circuit (the ΔI and ΔV starts the carrier before the distance unit picks up), via OR-16, S.Q. Timer (0/150 ms) and AND-50, to prevent the local transmitter from starting. (The receiver receives the signal from both local and remote transmitters.) At the same time, output of OR-40 will satisfy one input of AND-48 and also starts the channel coordination timer (BLKT), range 0 to 98, in 2 ms steps. (See **Segment 5.1.8e** for BLKT setting.) After the preset time of the channel coordination timer, logic AND-47 will satisfy AND-48, if there is no received carrier signal from either remote or local on internal faults,

and if the local transient block circuit (TBM) does not setup. Then AND-48 output will satisfy AND-52 and will produce pilot trip via OR-2 (**Figure 3-5**). Pilot trip target would be the same as for POTT.

(2) For a forward external fault, the local pilot relay (PLTP and/or PLTG) sees the fault, and operates in the same manner as for the forward internal faults. However, at the remote terminal, the carriers units ΔI/ΔV/ Z3P(R)/Z3G(R)/RDOG also sees this external fault and turns-on the transmitter via OR-41, AND-51, AND-50, OR-18, and AND-35, sending a blocking signal to the local and remote terminals. The local receiver receives the blocking signal, disables the operation of AND-47; therefore, AND-48 will produce no carrier trip signal for AND-52.

b. Carrier Keying Logic

(1) Reverse fault keying (**Figure 3-25**)

For a reverse fault, the ΔI and ΔV as well as the local reverse-looking relay Z3P(R)/ Z3G(R) or RDOG sees the fault, operates the CARSND relay and starts the transmitter, sending a blocking signal to the other terminals.

NOTE: T**he use of ΔI and ΔV for carrier start provides more security to the blocking scheme.**

This keying circuit includes logic OR-50A, AND-50, AND-173, OR-41, AND-51, OR-18 and AND-35. The signal of 52b to AND-35A is for disabling the “SEND” circuit when the breaker is open and line side potential is used.

Since the present keying practice on BLK system uses either the contact open (negative or positive removal keying) or contact close (positive keying) approach, a form-C dry contact output for keying is provided in MDAR.

(2) Signal continuation and TBM logic

For a reverse fault, both the local carrier start relay(s) and the remote pilot relay(s) see the fault and operate. The local carrier start relay(s) start the carrier and send a blocking signal to block the remote pilot relay from tripping. After the fault is cleared by the external breaker, the remote breaker may have a tendency to trip falsely if the carrier start unit resets faster than the pilot trip unit. The 0/50 ms timer between the OR-41D and AND-51 holds the carrier signal for 50 ms after the carrier start units have been reset for improving this problem. This logic also provides transient block and unblock (TBM) effect on power reversal.

The subsequent out-of-step condition (as described in **Section 3.4.17.1**), may cause the reverse looking units to fail to operate on external faults, and introduce false pilot tripping at the other end. Enhanced logic has been added to the design **as shown in Figure 3-25**, which includes OR-41C, 32/0 ms timer, AND-41B and OR-41. It utilizes the not FDOP (or FDOG) and LV condition (LV units can be set between 40 and 60 volts) to initiate the TBM circuit; and sends a blocking signal to the remote end. Set OSB to YES for supervising AND-41B when this enhanced logic is required in the application. Set WFEN to YES if this terminal may become a weak-feed condition.

(3) Internal fault preference and squelch

On an internal fault, the ΔI and ΔV signals also starts the transmitter for 65 ms. This operation may block the system from pilot tripping. The output signal from OR-40 to OR-16 to AND-50 and logic OR-16 to AND-120 will provide an internal fault preference feature for solving this problem. The squelch 0/150 ms timer is required for improving the problem if the local breaker tripped faster than the remote breaker on an internal fault. The logic disables the carrier key circuit (SEND) for 150 ms after any high speed tripping, including pilot trip, Zone-1 trip and instantaneous overcurrent trip.

c. Carrier Receiving Logic (**Figure 3-25**)

Carrier signal from the receiver output will be directly applied to AND-47 to disable the pilot tripping function.

d. Channel Indication (not shown in **Figure 3-25**)

Since the carrier channel turns “ON” for external faults only, the channel indicators (SEND and RCVR) should not be sealed-in.

e. Channel Simulation

Same as for POTT scheme.

f. Programmable Reclosing Initiation (**Figure 3-19)**

Same as for POTT scheme.

3.5.4 High Resistance Ground Faults - Pilot Supplement

Pilot ground is more dependable on high resistance faults because it is supplemented with FDOG and IOM (**refer to Figure 3-26**).

Supplemental protection is provided on overreaching pilot systems to detect high resistance ground faults. The instantaneous forward directional overcurrent ground function (FDOG) works in conjunction with the pilot ground distance unit. The FDOG directional unit is determined by the setting of DIRU (ZSEQ/NSEQ/DUAL). **Refer to Section 3.4.11** for the setting of DIRU. FDOG is supervised by the IOM setting. A coordination timer FDGT (T/0) is provided to allow preference for pilot ground distance (mho) unit operation. The delay time (T) can be set from 0 to 15 cycles in 1 cycle steps. It is recommended to set the FDGT timer to 3 cycles or longer for security reasons.

3.5.5 Power Reversal on POTT

Pilot ground is more secure on POTT/unblocking schemes on some special power system conditions, such **as shown in Figure 3-27**. A $\phi\phi$G fault is on the paralleled line section. Due to the system condition, fault current flows in the protected line would be I1+I2 from A to B, and Io from B to A. The operation of pilot distance relays would be a phase relay at A and a ground relay at B. The result would be erroneous directional comparison of an external fault as an “internal” one. The POTT/unblocking scheme will incorrectly trip out of the protected line.

MDAR POTT/Unblocking pilot ground unit (PLTG/FDOG) is supervised by the reverse-looking ground unit (RDOG). The “Reverse-Block” logic is **as shown in Figure 3-32**. At terminal A, the RDOG disables the PLTG/FDOG trip/key functions via OR-9A, AND-45A AND-45 and AND-30. At terminal B, it will receive no carrier signal for permissive trip. The reverse-block logic also provides the conventional TBM feature to prevent false operation on power reversal. It should be noted that a “Block-the-Block” logic is also included in the circuit, **as shown in Figure 3-32**. The Block-the-Block logic is to prevent the Reverse-Block logic from over-blocking (*see the following system condition*). If the breaker is unequal-pole closing on a ϕG fault, say pole-A, pole B and C close at a later time (**refer to Figure 3-28**). If, due to breaker contact asymmetry, the first breaker contact to close is the one of the faulted-phase, the zero-sequence (or negative sequence) polarizing voltage will initially have a polarity opposite to its fault-derived polarity, the reverse-looking ground unit could pick-up for a short period, issue a blocking order, and maintain it for 50 ms consequently, the correct tripping will be delayed. The Block-the-Block logic would prevent this delaying. The Reverse-Block logic also includes the reverse looking Z3P/Z3G units **as shown in Figure 3-32.**

3.6 3-ZONE DISTANCE PHASE AND GROUND WITH INDEPENDENT PILOT PHASE AND GROUND

There are four impedance units per zone: one phase-to-phase unit and three phase-to-ground units (**see Section 3.3**). The following table shows the role of each distance unit per pilot zone scheme.

Distance Units			
Scheme	Z1P/Z1G	Z3P/Z3G (Reverse)	PLTP/PLTG
POTT/		Block	
UNBLOCK		Pilot Trip	Key/Trip
PUTT	Start Key	----	Trip
BLOCK	----	Start Key	Trip and Stop Key

NOTE: Beyond pilot logic functions, Z1P/Z1G and Z3P/Z3G perform basic Zone-1 and Zone-3 functions. Z2P/Z2G function is independent. For Pilot system application Z3FR has to be set to REV. Set T3P = T3G = BLK if Zone-3 trip is not used.

3.7 INVERSE TIME DIRECTIONAL OR NON-DIRECTIONAL (SELECTABLE) OVERCURRENT GROUND BACKUP.

(**See Section 3.4.2**)

3.8 INSTANTANEOUS REVERSE DIRECTIONAL OVERCURRENT GROUND FUNCTION.

Similar to FDOG, the instantaneous reverse directional overcurrent ground function (RDOG) supplements the pilot zone logic.

3.8.1 Supplement to Reverse Z3G Trip.

In the blocking system, RDOG, supervised by IOS, provides additional ground fault detection (high resistance) beyond what is available by Z3G (reverse looking) for carrier start.

3.8.2 Carrier Ground Start on Blocking Scheme

In the POTT/UNBLOCK systems, RDOG supervises PLTG and prevents keying or tripping on reverse faults.

3.8.3 Weakfeed System Application

For weakfeed applications, an inherent part of the logic requires reverse fault detection; Z3P/Z3G and RDOG supply this requirement.

3.9 LOSS-OF-POTENTIAL SUPERVISION (LOP, See Section 3.4.3)

3.10 LOSS-OF-CURRENT MONITORING (LOI, See Section 3.4.4)

3.11 OVERCURRENT SUPERVISION (See Section 3.4.5)

3.12 INSTANTANEOUS OVERCURRENT TRIP (See Section 3.4.6)

3.13 HIGH-SET INSTANTANEOUS DIRECT TRIP, INCLUDING THREE-PHASE AND ONE GROUND OVERCURRENT UNITS FOR SPT/3PT APPLICATION (See Section 3.4.6)

3.14 CLOSE-INTO-FAULT TRIP AND STUB BUS PROTECTION (See Section 3.4.7)

3.15 UNEQUAL-POLE CLOSING LOAD PICKUP LOGIC (See Section 3.4.8)

3.16 SELECTABLE LOSS-OF-LOAD ACCELERATED TRIP LOGIC (LLT) (See Section 3.4.9)

3.17 CURRENT CHANGE FAULT DETECTOR (See Section 3.4.10)

3.18 VOLTAGE CHANGE FAULT DETECTOR (See Section 3.4.10)

3.19 3-TERMINAL LINE APPLICATION

For a 3-terminal BLK application, since the frequency of the three transmitters are the same, any one transmitter starting will block the pilot system from tripping, therefore, logic for the 3-terminal BLK pilot system would be the same as that used for the 2-terminal BLK system. However, for POTT/PUTT/UBLK systems, since the transmitter frequency is different at each terminal, logic for the second receiver (RCVR-2) should be added to the system when the application involves 3-terminals. Functional display “3TRM” should be set at “YES” position when the 3-terminal line is applied.

a. Additional Logic For POTT and Simplified Unblocking (**Figure 3-29**)

This logic includes contact converters (CC) for RCVR-2, AND-55, and logic for the second receive indication. The second receiver output operates the contact converter (or voltage). Output of AND-55 provides carrier trip signal (CR) to satisfy AND-30 via AND-64 and allows pilot tripping.

b. Additional Logic for PUTT (**Figure 3-30**)

The additional logic for this scheme would be similar to that as described for POTT scheme, except logic includes AND-56, AND-57 and 50/ms timer. This is because only the Zone-1 reach relay keys the transmitter on internal faults. For a close-in Zone-1 fault, only the local terminal can key its transmitter and the other two cannot. This logic provides a CR pilot trip signal for 50 ms for system security. For a fault which can be detected by relays at two terminals, AND-55 logic can be satisfied, then pilot trip will be performed via the logic in the usual way.

3.20 WEAKFEED TRIP APPLICATION

a. Block/Weakfeed

The logic for a weakfeed terminal is not required for the BLK system because the BLK system requires no permissive trip signal from the remote end, even though the remote end is a weakfeed terminal. The

strong end has no problem tripping for an internal fault. The weak end is usually assumed either as a "no feed" source, for which it does not need to trip on an internal fault, or it can pilot trip sequentially.

NOTE: Refer to Figure 3-25, logic AND-41B and OR-41C, WFEN should be set to YES if OSB is set to YES and this terminal may become a weak condition.

For the bench test, at the conditions of V = 0 and I = 0, the carrier keying contacts will be closed for the settings of OSB = YES and WFEN = NO. In an actual system, 52b will be applied to OR41C, because of V = 0 and I = 0, and the carrier keying signal will not be sent.

b. PUTT/Weakfeed

The logic for a weakfeed terminal is not required for the PUTT system. Because the PUTT system uses underreaching relay(s) only for pilot trip keying, it is impossible to apply this scheme to protect a system which may have weakfeed condition.

c. POTT/ Weakfeed

For POTT and unblocking schemes, at the weak source terminal, the Z3P/Z3G distance relays should be set for reverse-looking, and the undervoltage units (LVA, LVB, LVC) should be used. The basic operating principle of the weakfeed trip logic for the POTT and simplified unblocking scheme is as follows:

(1) Echo key for trip permission (**Figure 3-31**)

On internal faults, the strong source end sends the trip (or unblocking) frequency signal to the weak end, and its pilot trip relay(s) will trip, once it receives echo trip permission from the weak end. The pilot trip relay(s) at the weak end cannot pick up due to not enough internal fault energy, and does not perform the normal keying function. With one weakfeed condition, when the weak end receives a trip or unblocking signal, the output from the receiver operates the echo key logic AND-65, providing both pilot relay (from OR-40) and reverse-looking relay (from OR-41A) do not pick-up, and if system disturbance is detected (ΔV or ΔI). Output of AND-65 will key the weak terminal transmitter to the trip or unblocking frequency via OR-18, AND-35. On weak end reverse external fault, the strong source end sends the trip (or unblocking) frequency signal to the weak end, and its pilot trip relay(s) is waiting to receive the echo trip permission from the weak end. However, at the weak end, the echo key logic AND-65 will not operate, because of the reverse looking relay operation, it sends no echo signal to the strong end. Both the strong/weak ends will not trip on this external fault.

(2) Weak end trip on internal fault (**Figure 3-31**)

The output of AND-65 (start echo keying) together with no output from OR-40 (pilot trip relays), and with output from OR-44 (low voltage condition) will satisfy AND-66; weakfeed trip will be performed after 50 ms via OR-2. The timer delay is for coordination because the voltage trip units are non-directional.

3.21 LOGIC FOR RB ON BF SQUELCH (Setting BFRB)

For a pilot system, the BFI signal can be used to stop (for a blocking system) or start (for permissive schemes) the carrier channel to allow far end line terminals to trip in the event a breaker close to an external fault fails to open. The problem is how to inhibit reclosing on those terminals, to limit damage.

MDAR solves this problem at the far end terminals by the Reclose Block on Breaker Failure Squelch logic in the RI/RB software. When the breaker fails to trip, the BFI logic squelches the channel to continuous permissive signal, or stops the blocking signal. This is done after some time delay. The relay at the far end, having sensed the external fault in the forward direction, sees the permissive signal (or stoppage of blocking signal) much later than it would for a normal pilot trip operation initiated by relay forward-looking elements at the end closer to the fault. This time delay is used to differentiate between a faster normal pilot trip and the slower problem-related pilot trip initiated by BFI, and to block reclosing in the latter case.

This logic is shown in **Figure 3-19**, which includes AND-61A and a 132/0 ms timer. The logic at the far end terminal will initiate RB (and inhibit RI) at 132 ms (about eight cycles) after the fault is detected by the overreaching PLTP or PLTG element, if the pilot is

enabled and the TRSL signal is received on any three-pole trip operation. If the fault is cleared before the 132 ms expiration of the timer, normal reclosing will occur.

3.22 OUT-OF-STEP (OS) LOGIC (Refer to Section 3.4.17)

3.23 OPTIONAL SINGLE-POLE TRIP (SPT) LOGIC AND OUTPUTS (Refer to Section 3.4.18) Without Programmable Output Contact Option

3.24 OPTIONAL PROGRAMMABLE OUTPUT CONTACTS WITHOUT SPT OPTION

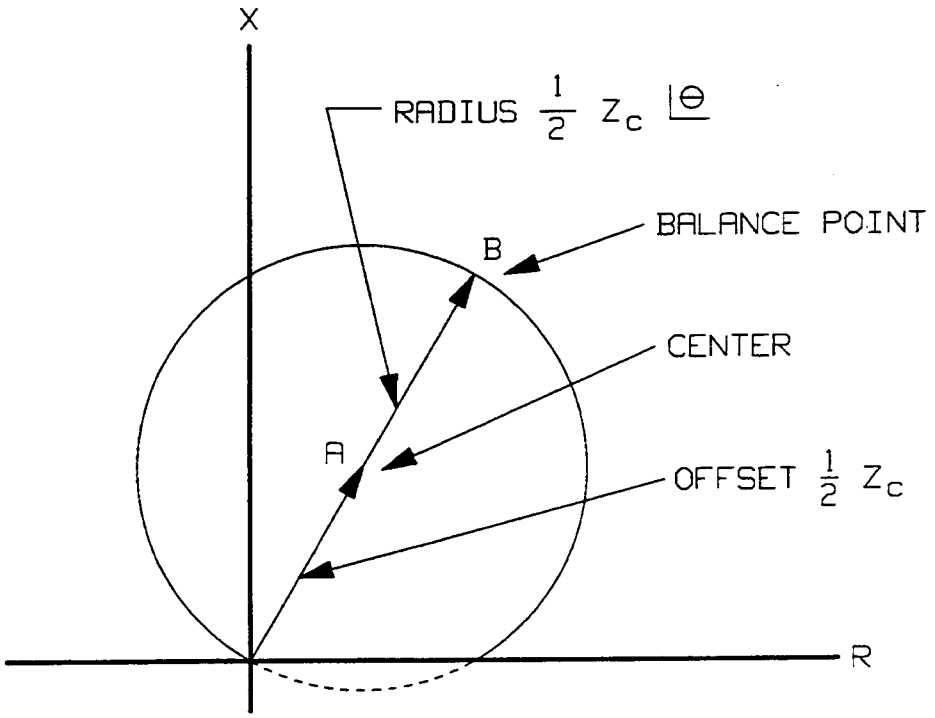
The optional programmable output contact module consists of 8 relays, 4 with heavy duty NO contacts (OC1 to OC4) and 4 with standard contacts (OC5 to OC8) with jumper selection for NO or NC outputs. Contacts OC4 and OC8 provide timers for delay pickup and/or delay dropout. The ranges of timers are 0 to 5 seconds in 0.01 second steps with an error of $\pm$ 1 cycle. Every Contact (OC1 to OC8) can be programmed independently based on one or all of the 30 pre-assigned signals with AND/OR logic combination. These 30 signals are listed in **Table 3-4** and **Figure 3-33**. All 8 output settings can only be performed through remote WRELCOM® communication.

In addition to the foregoing features and options, the MDAR Pilot Zone system includes many of the same special functions as the Non-Pilot system, i.e.:

- RS-232C port (**See Sections 4.3 and 4.7**).
- Line voltage, current and phase angle monitor (**See Section 4.4.2**).
- Reclosing initiation and reclose block outputs. **Refer to Section 5.3** for RI Guidance, except set the relay to PLT = YES and apply a rated voltage to PLT/ENABL terminals TB5/9(+) and TB5/10(-).
- Fault Locator function, and current change fault detector (**See Section 1.5**).
- Self-check function (**See Section 1.6**).

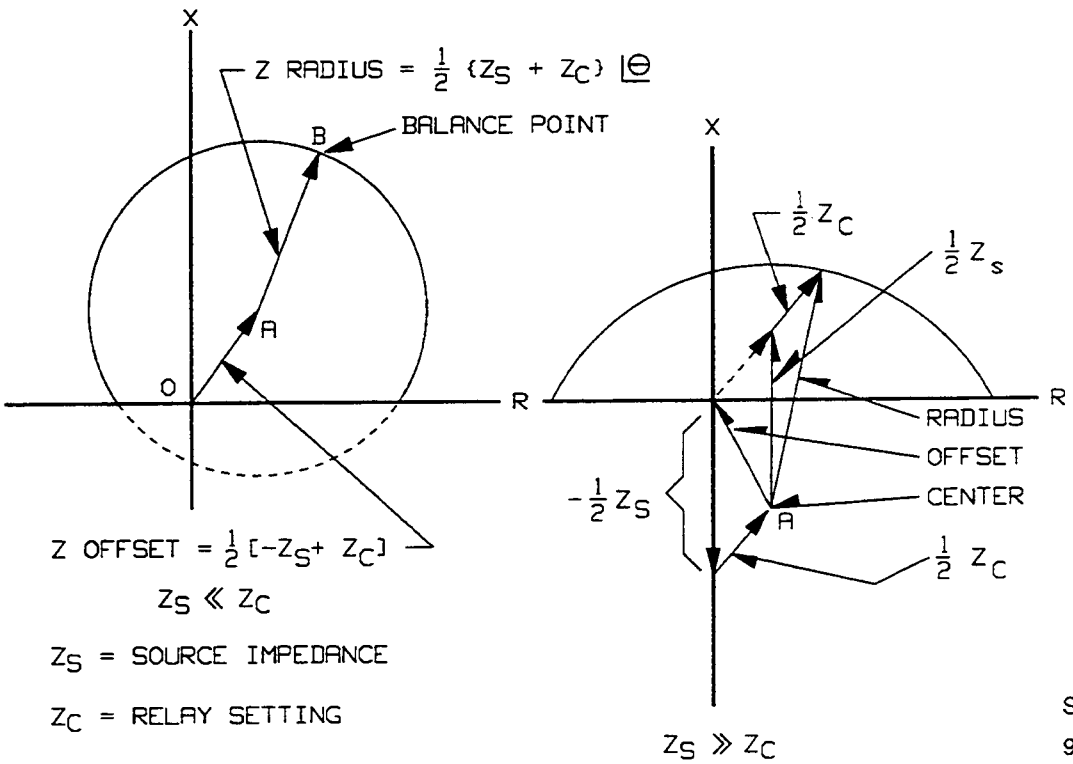
3.25 MDAR Ordering Information

The MDAR equipment is identified by the Catalog Number on the MDAR nameplate which can be decoded by using **Table 3-1**.



Sub 1
9654A14

Figure 3-3 Mho Characteristics for Three-Phase Faults (No Load Flow).



Sub 1
9654A15

Figure 3-4 Mho Characteristics for Phase-to-Phase and Two Phase-to-Ground Faults (No Load Flow).

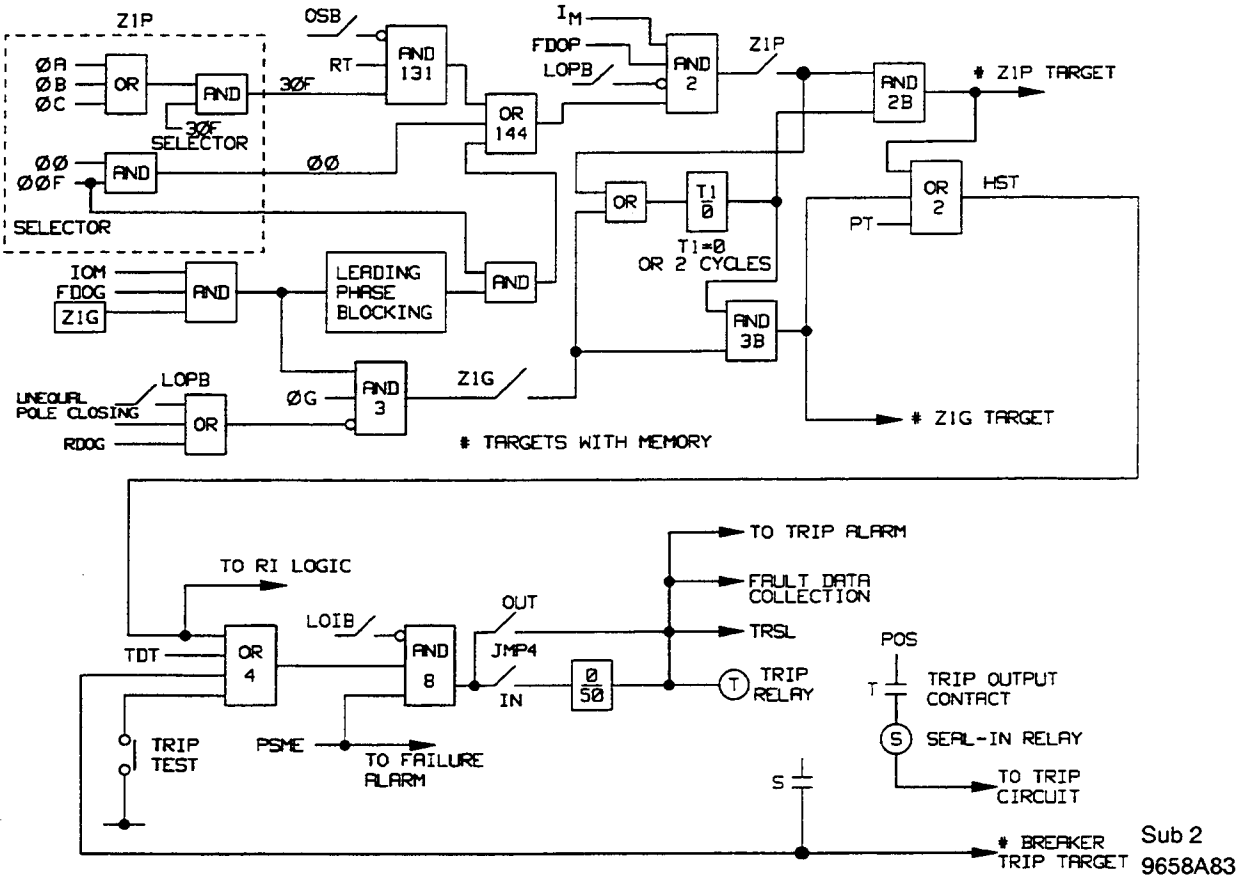


Figure 3-5 MDAR Zone 1 Trip Logic.

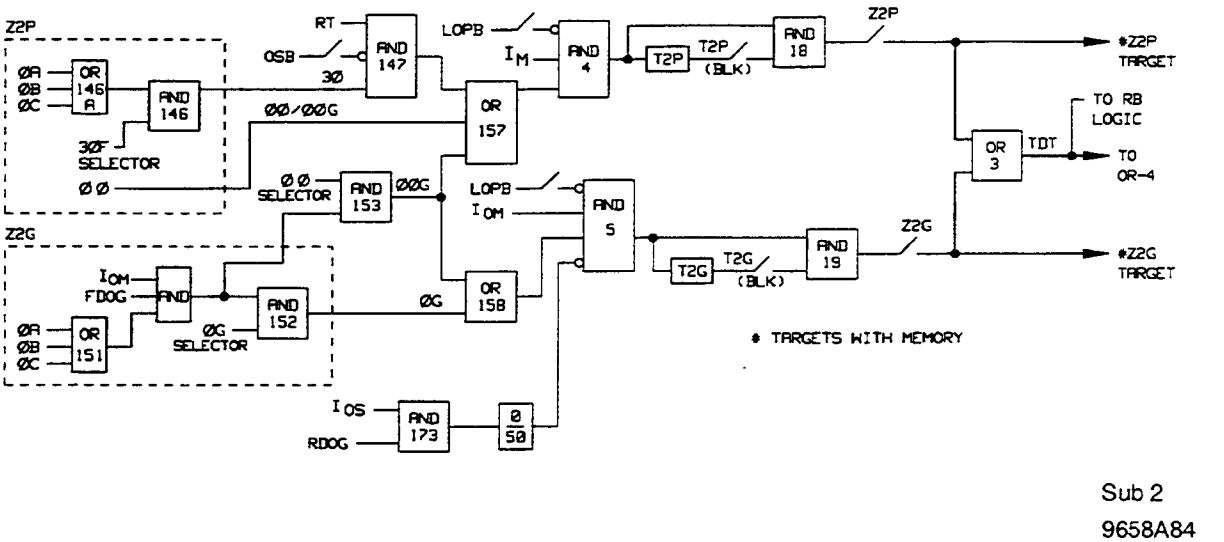


Figure 3-6 MDAR Zone 2 Trip Logic.

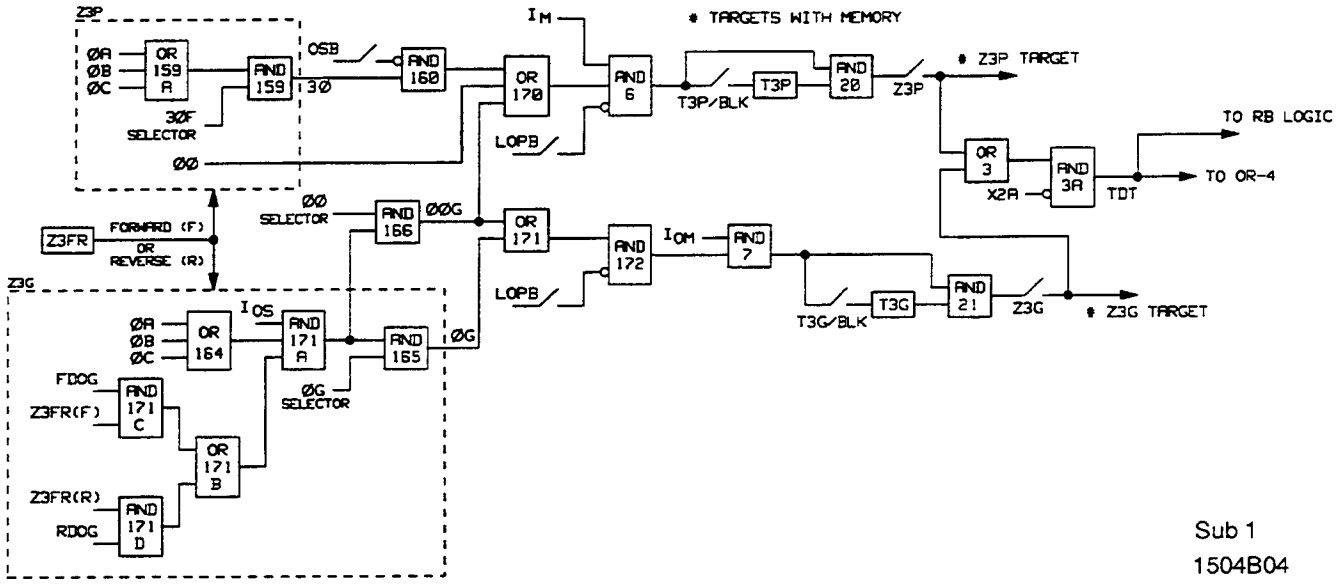


Figure 3-7 MDAR Zone 3 Trip Logic.

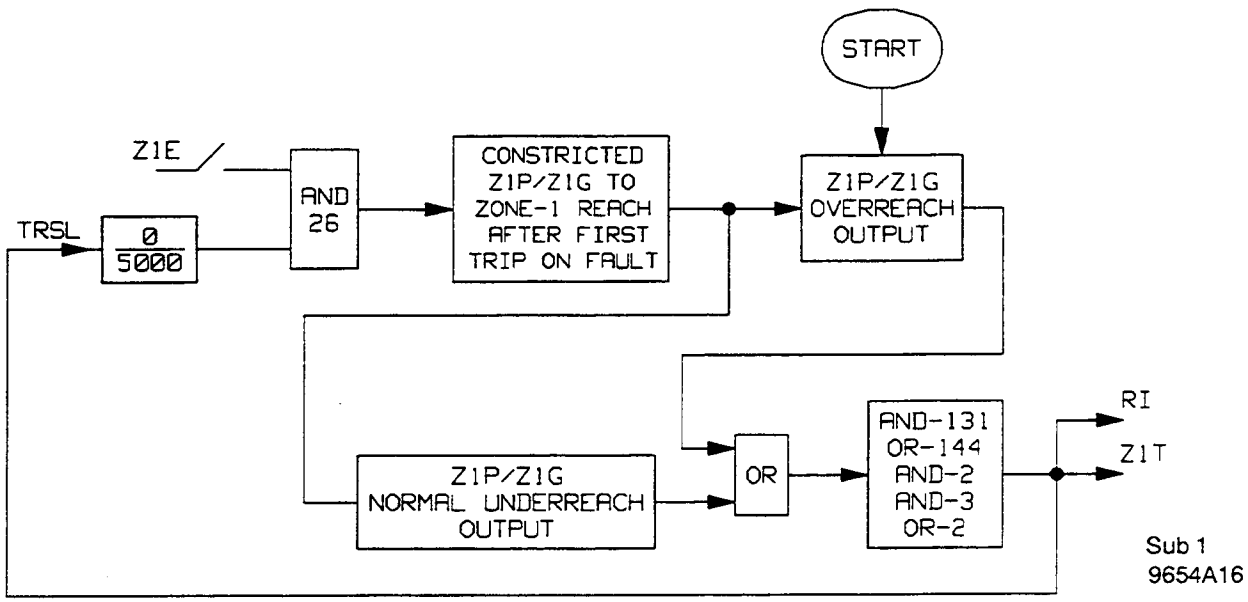


Figure 3-8 MDAR Zone 1 Extension Scheme.

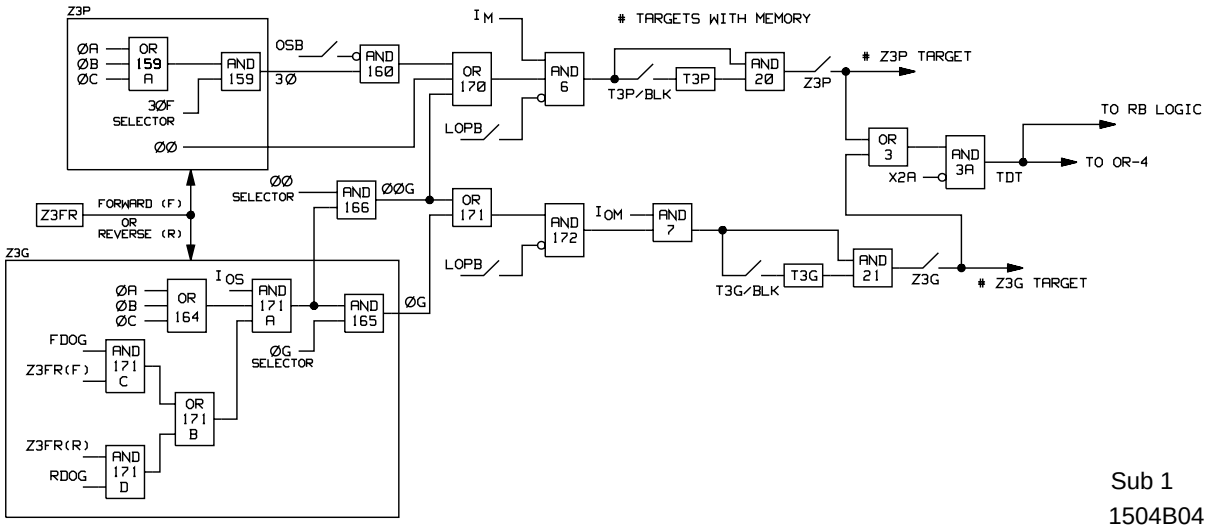


Figure 3-7 MDAR Zone-3 Trip Logic.

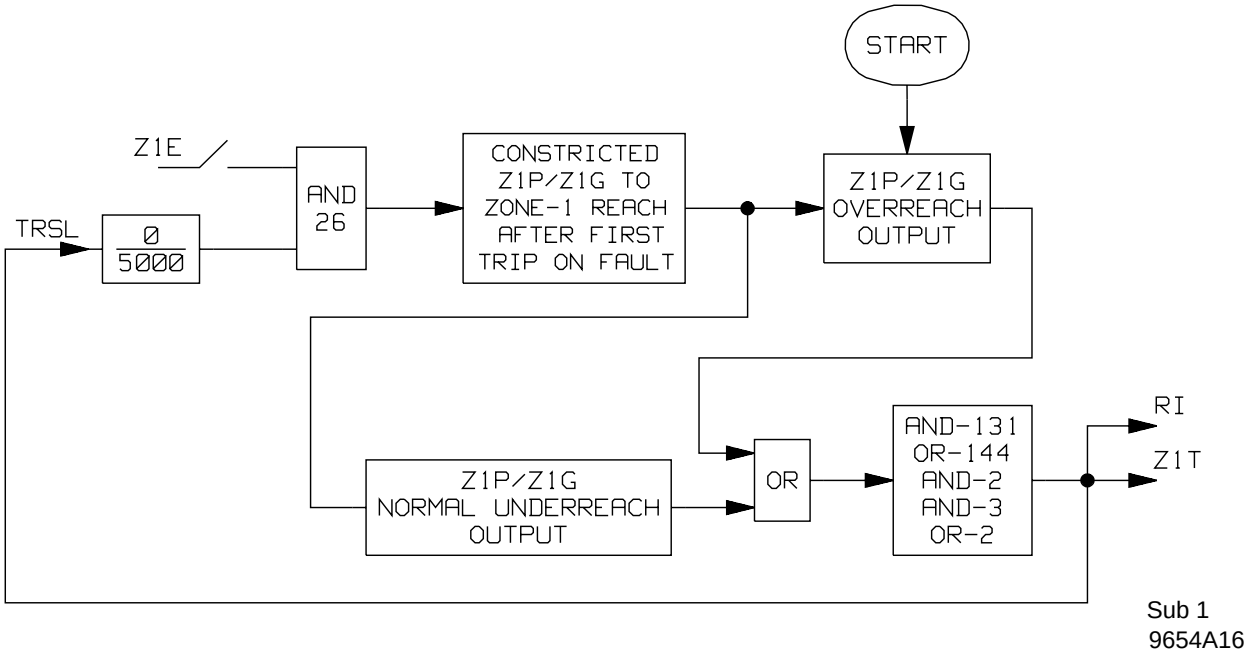


Figure 3-8 MDAR Zone-1 Extension Scheme.

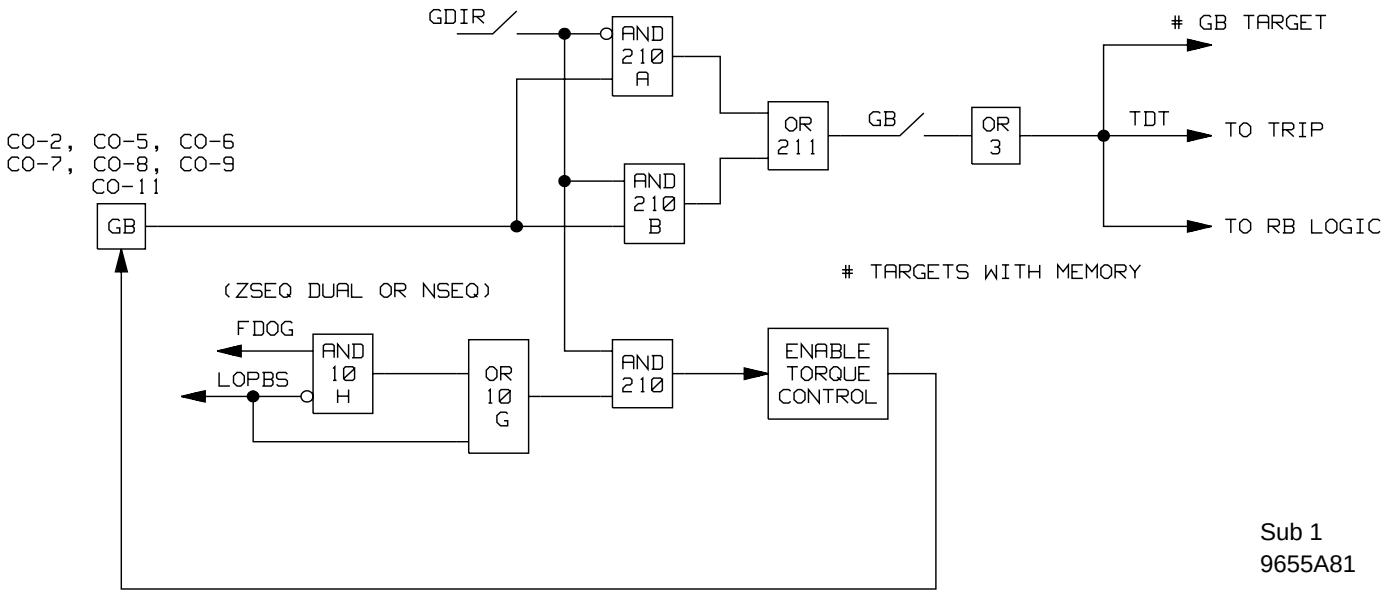


Figure 3-9 Inverse Time Overcurrent Ground Backup Logic.

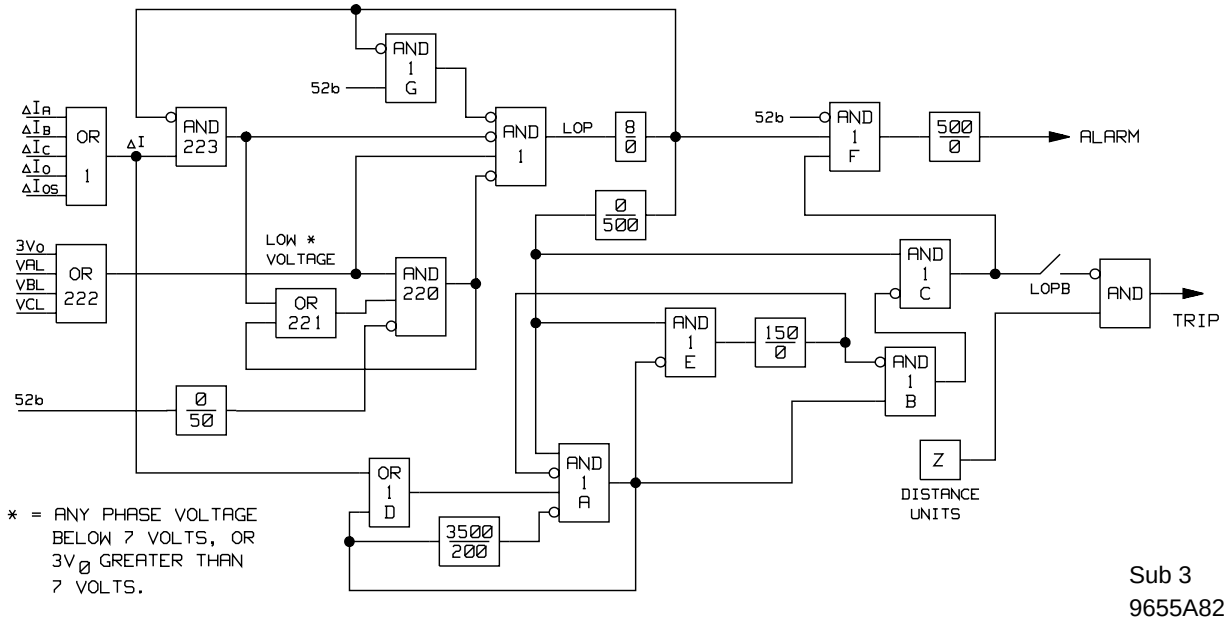


Figure 3-10 Loss-of-Potential Logic.

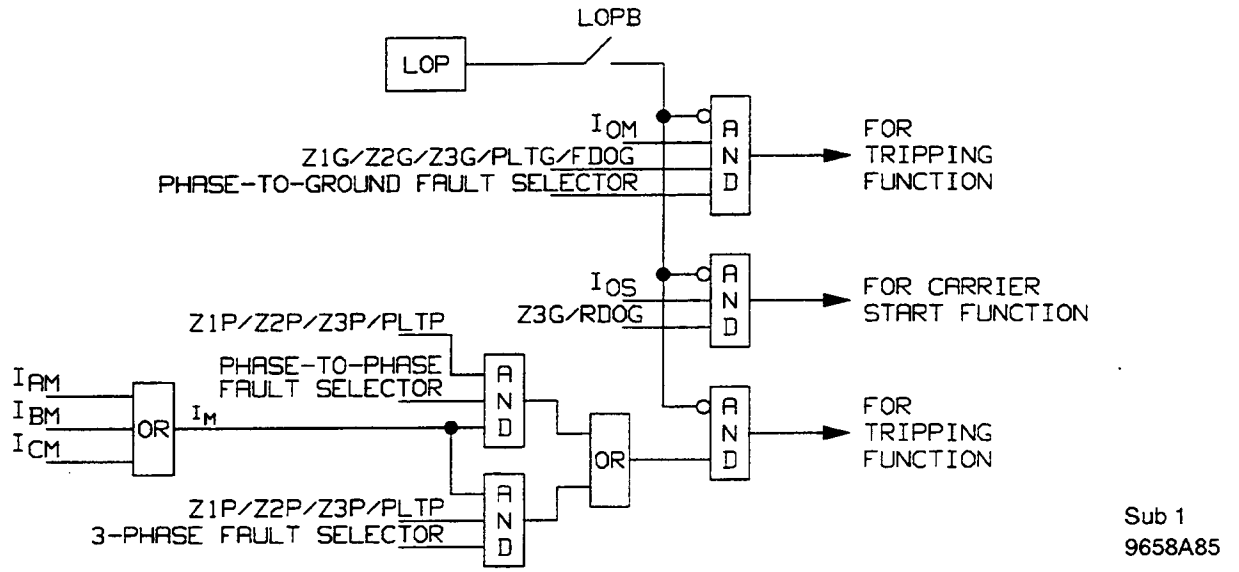


Figure 3-13 Overcurrent Supervision.

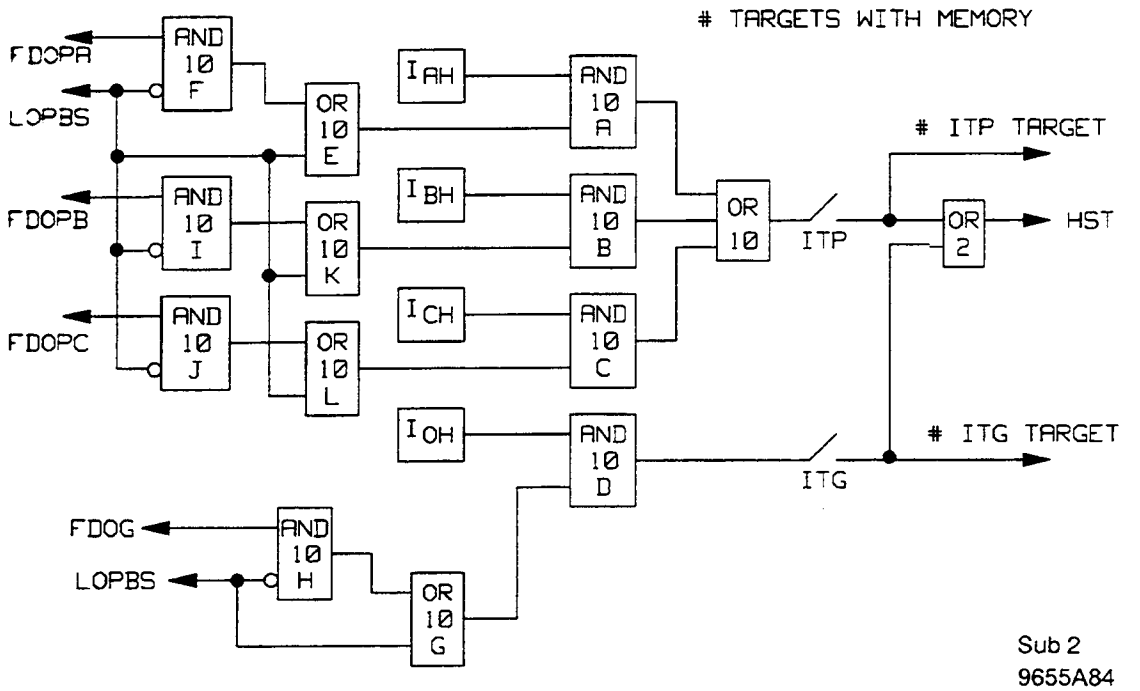


Figure 3-14 Instantaneous Overcurrent Highset Trip Logic.

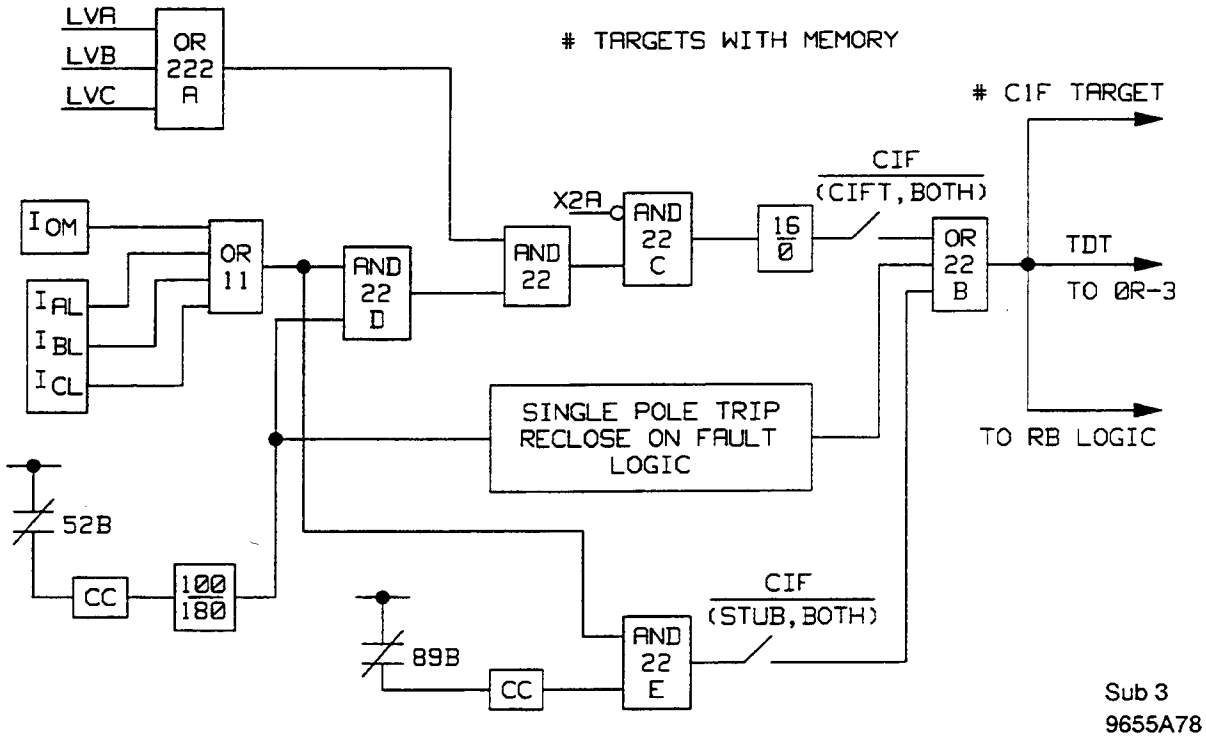


Figure 3-15 MDAR Close-Into-Fault Trip (CIFT) and Stub Bus Protection Logic.

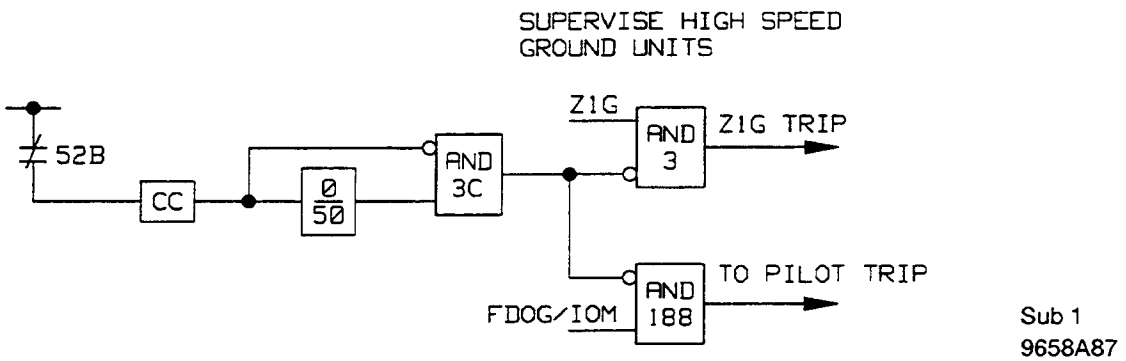


Figure 3-16 MDAR Unequal-Pole-Closing Load Pickup Trip Logic.

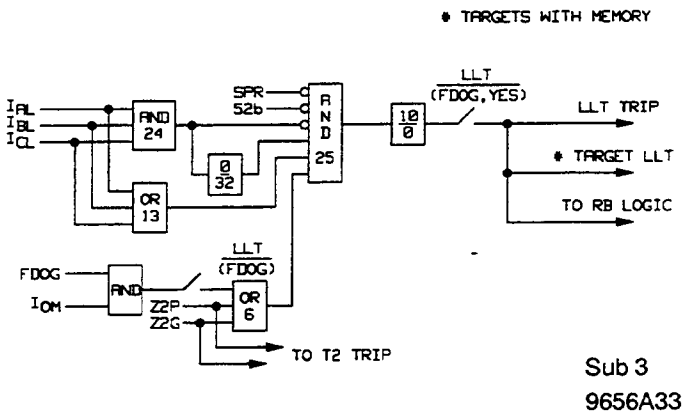


Figure 3-17 Load Loss Accelerated Trip Logic.

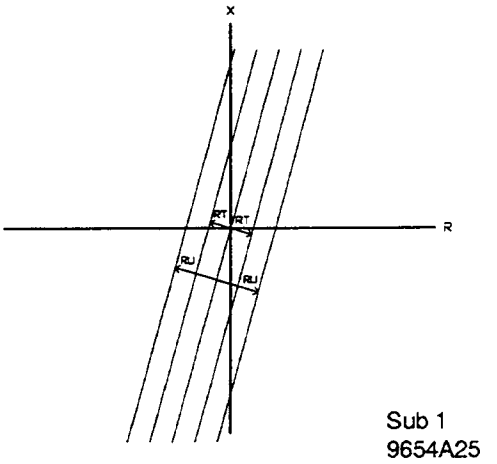


Figure 3-18b Out-of-Step Block Logic (Blinder Characteristics).

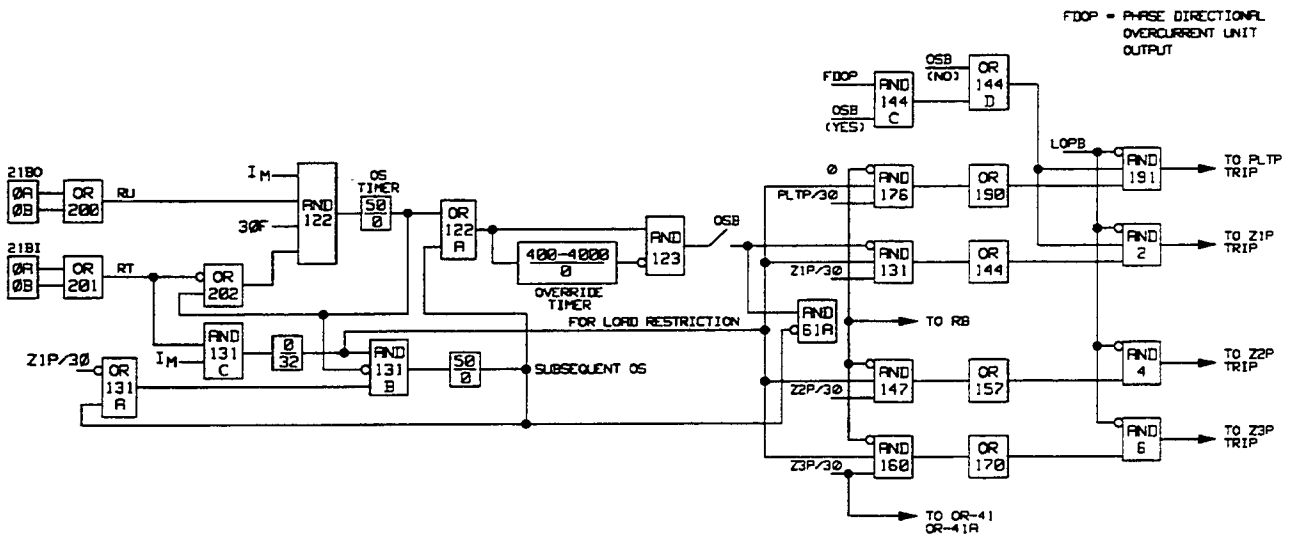
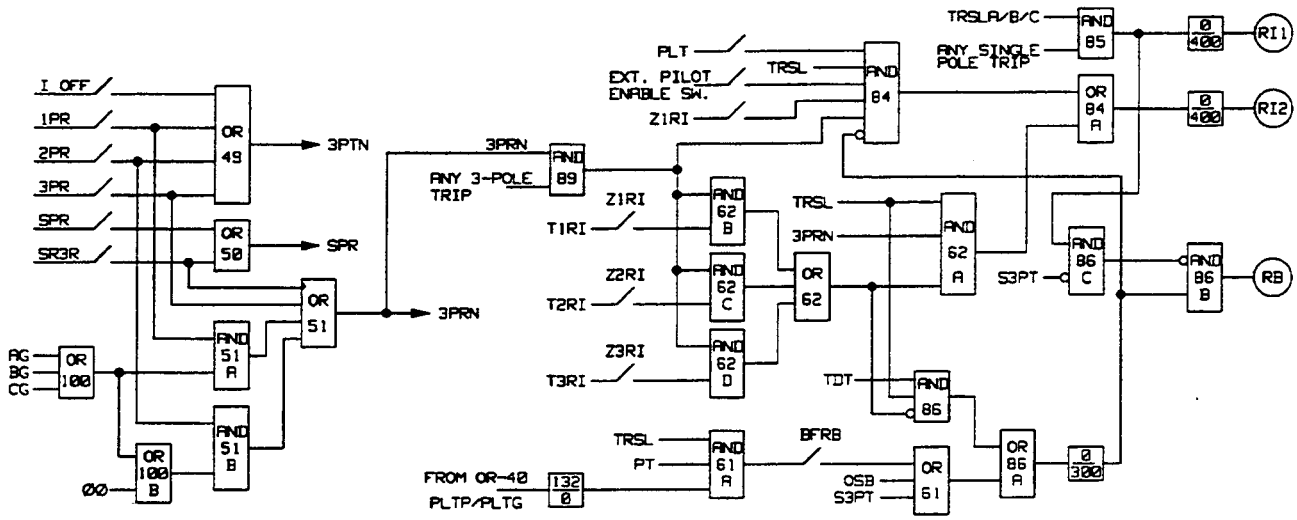
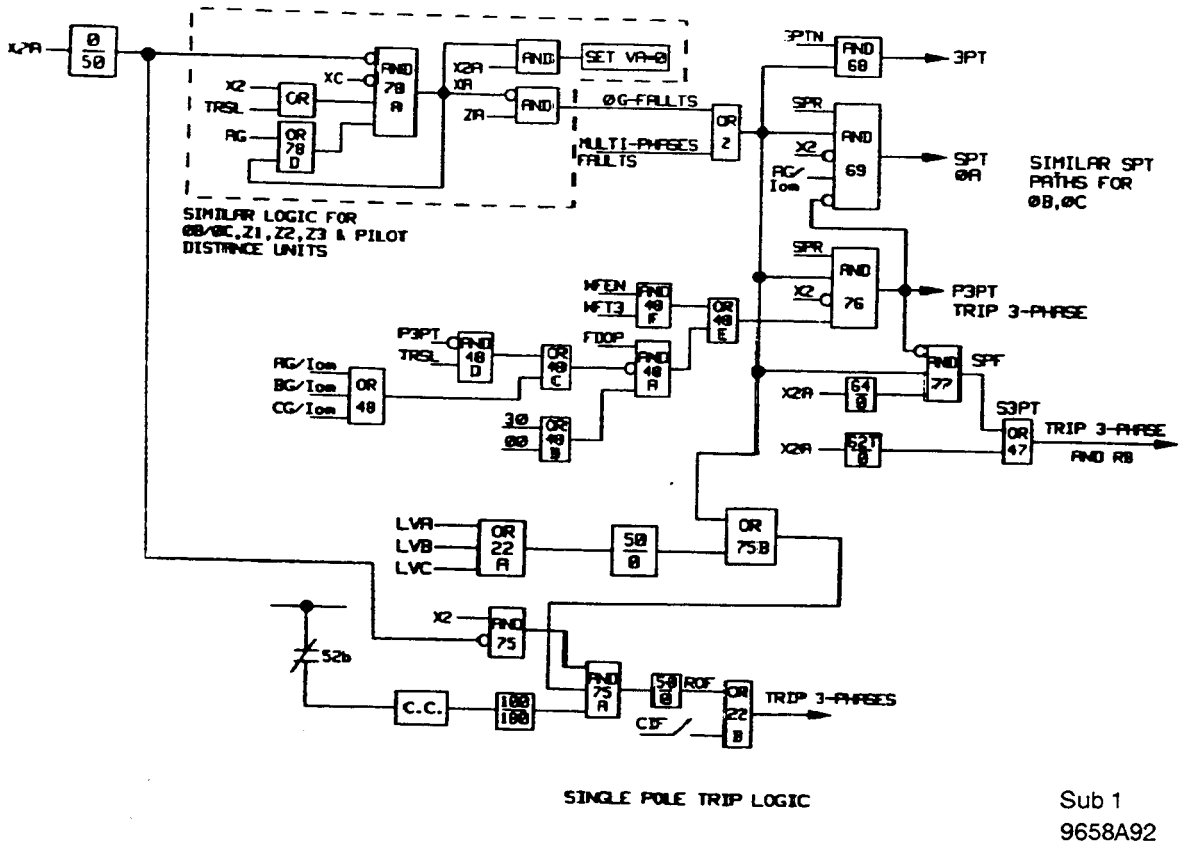


Figure 3-18a Out-of-Step Block Logic.



Sub 5
1501B86

Figure 3-19 Reclosing Initiation Logic.



Sub 1
9658A92

Figure 3-20 Single Pole Trip Logic.

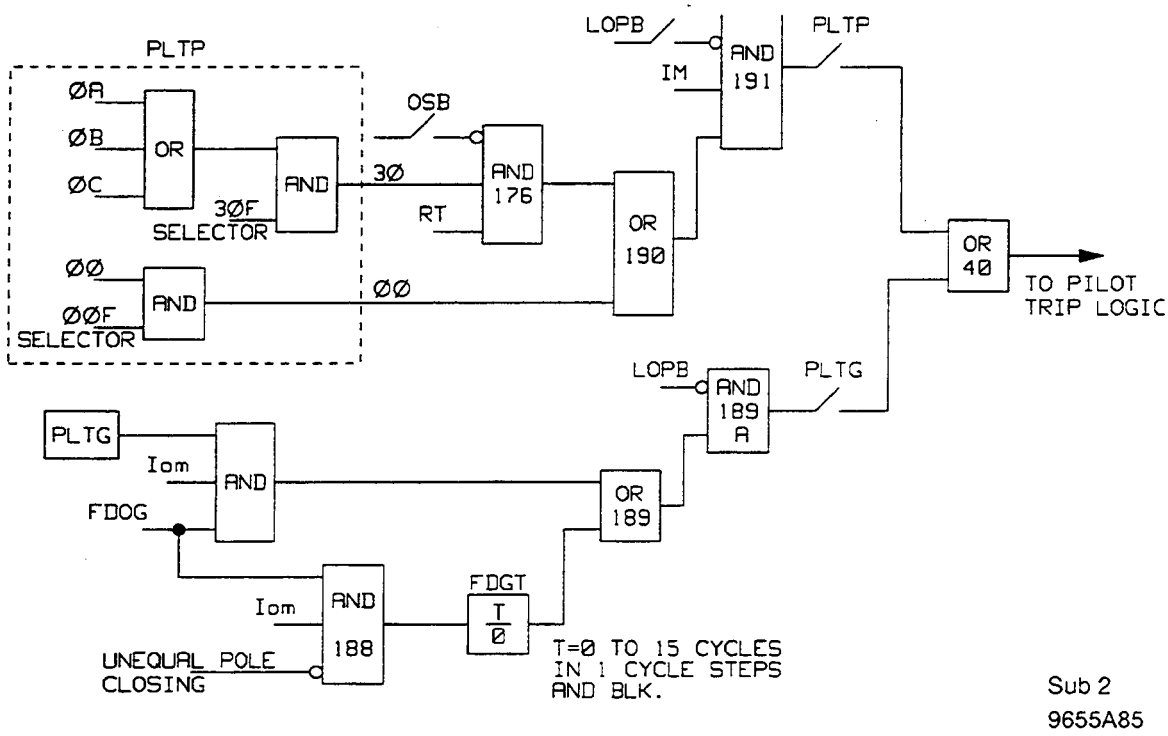


Figure 3-21 Pilot Trip Relay.

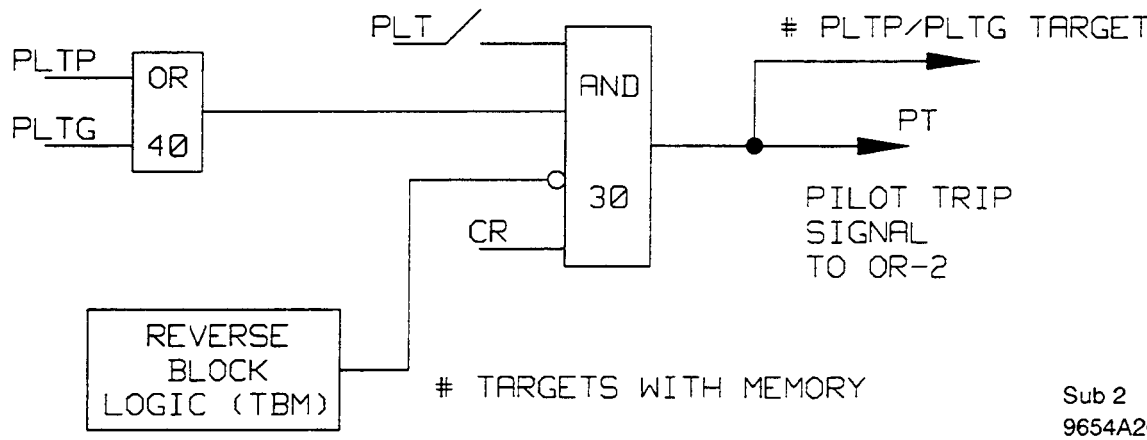


Figure 3-22. POTT/Unblocking Pilot Trip Logic.

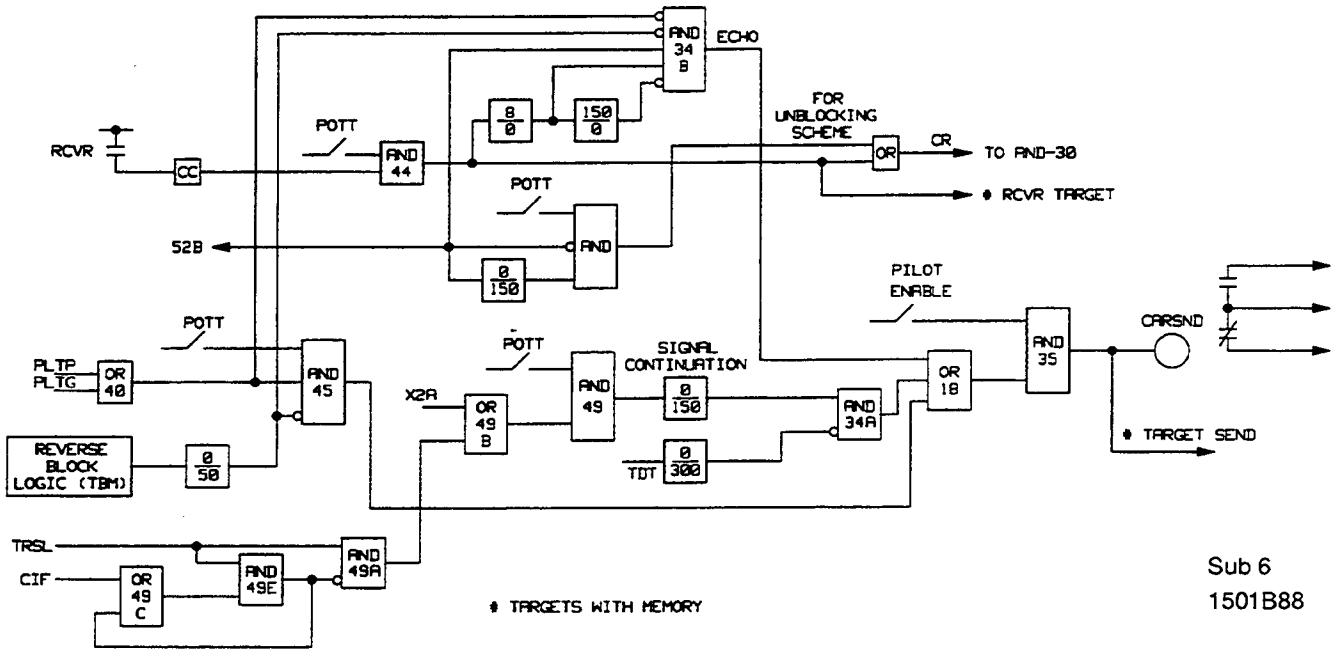


Figure 3-23 Carrier Keying/Receiving Logic in POTT/Unblocking Schemes.

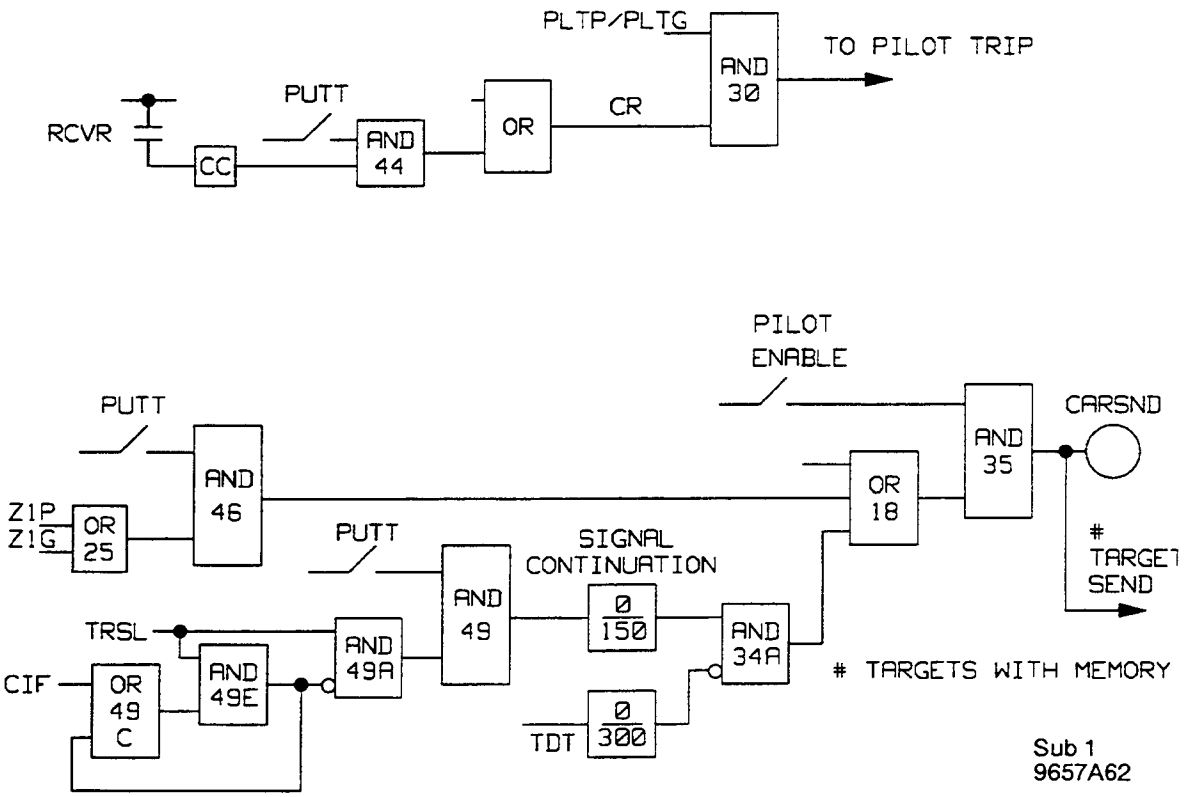


Figure 3-24 PUTT Keying Logic.

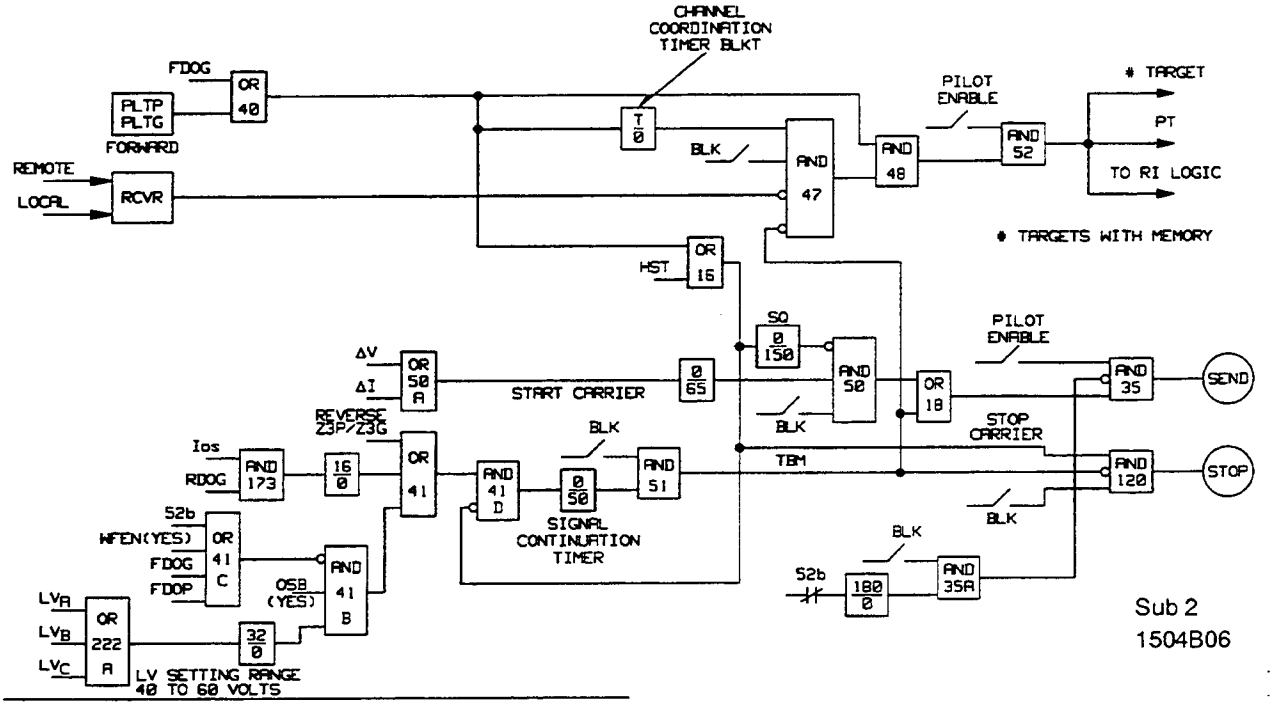


Figure 3-25 Blocking System Logic.

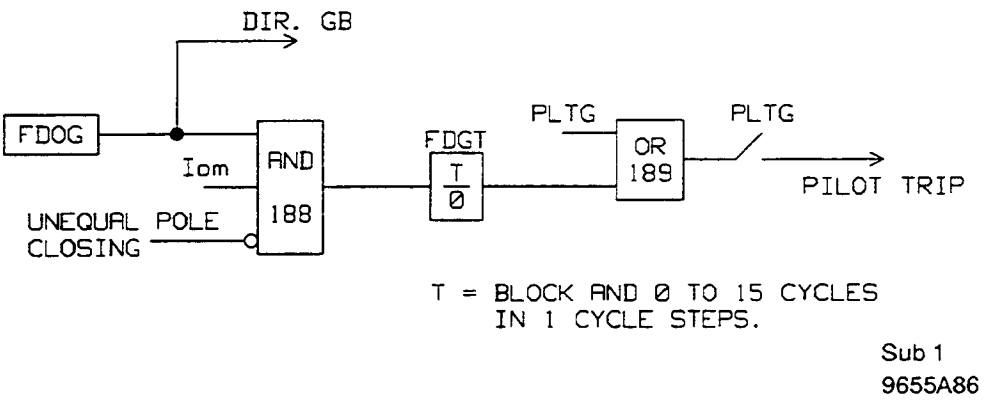


Figure 3-26 PLTG Supplemented by FDOG.

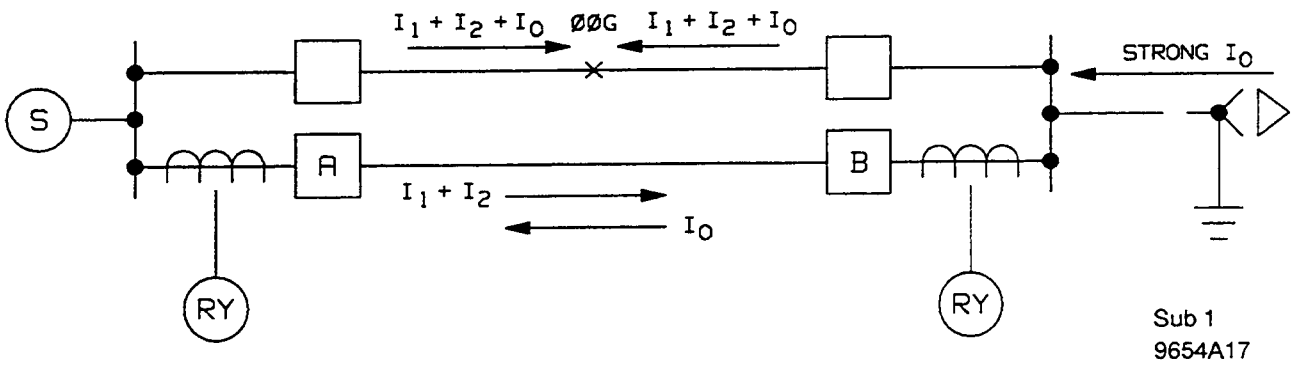


Figure 3-27 Power Reversed on POTT/Unblocking Schemes.

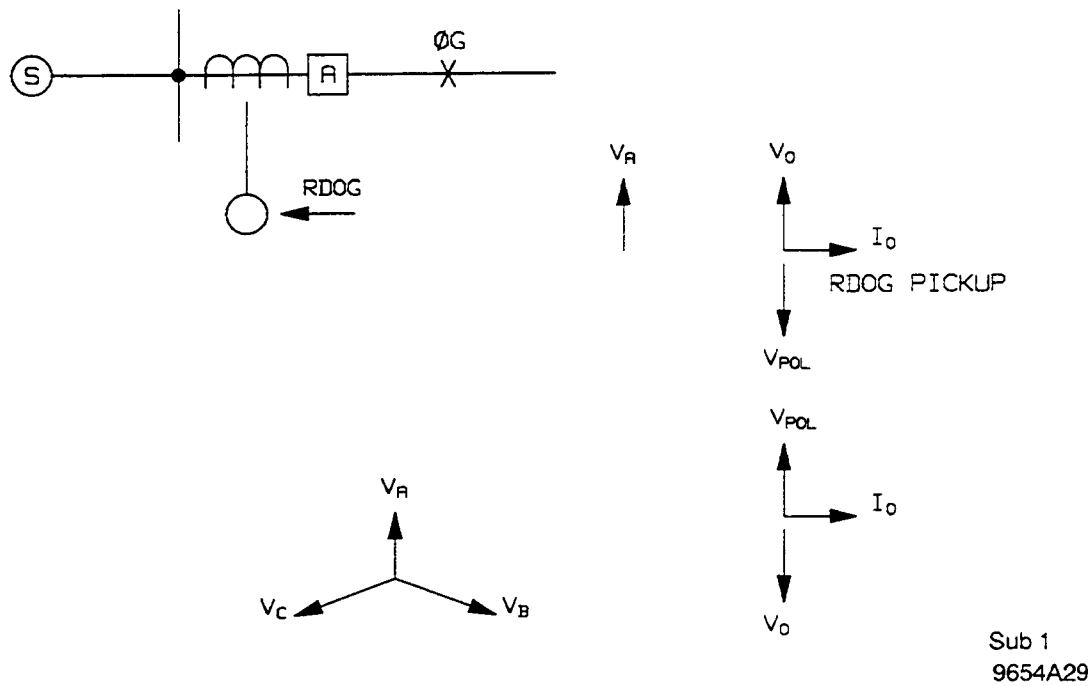
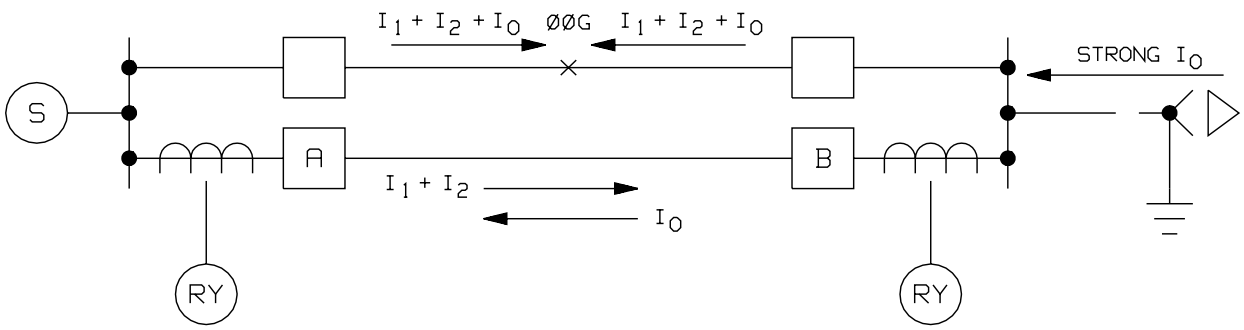
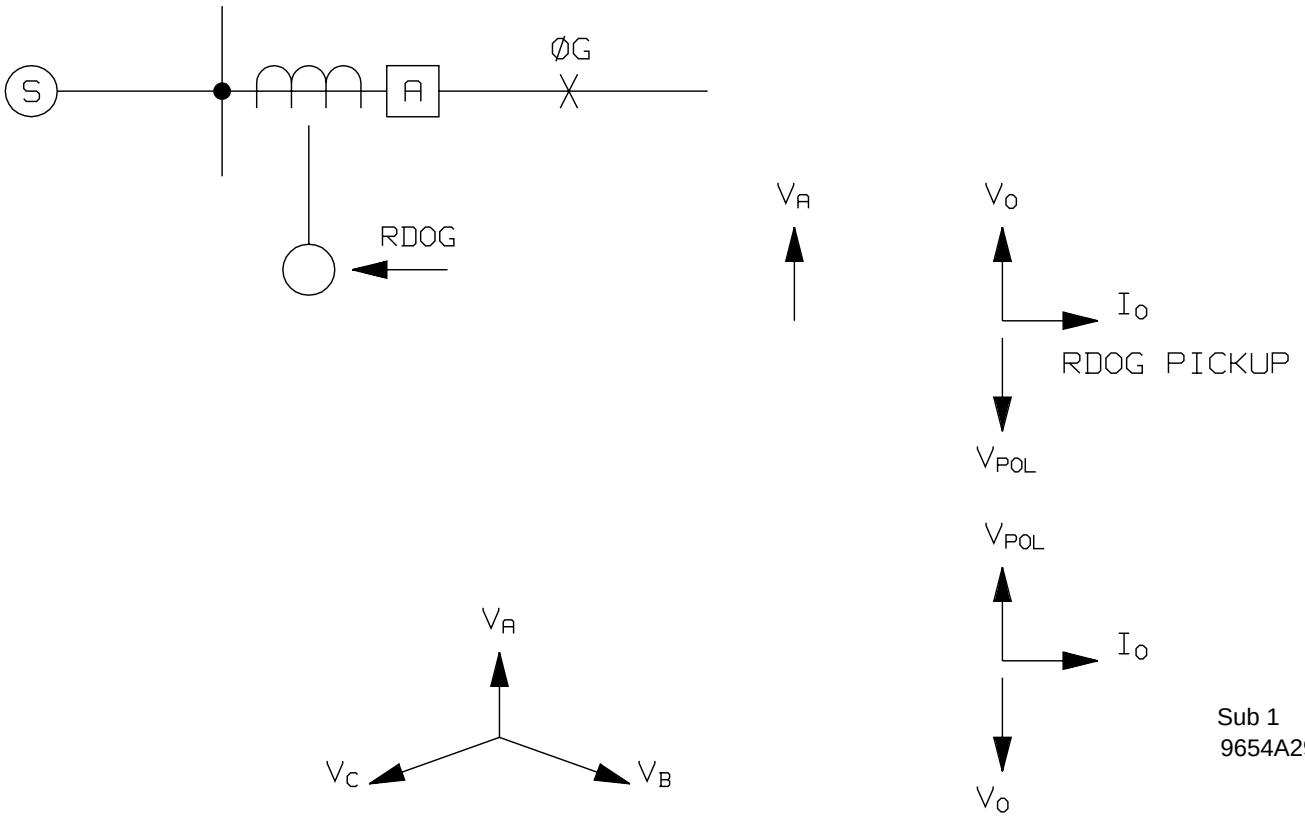


Figure 3-28 Unequal Pole Closing on Fault.



Sub 1
9654A17

Figure 3-27 Power Reversed on POTT/Unblocking Schemes.

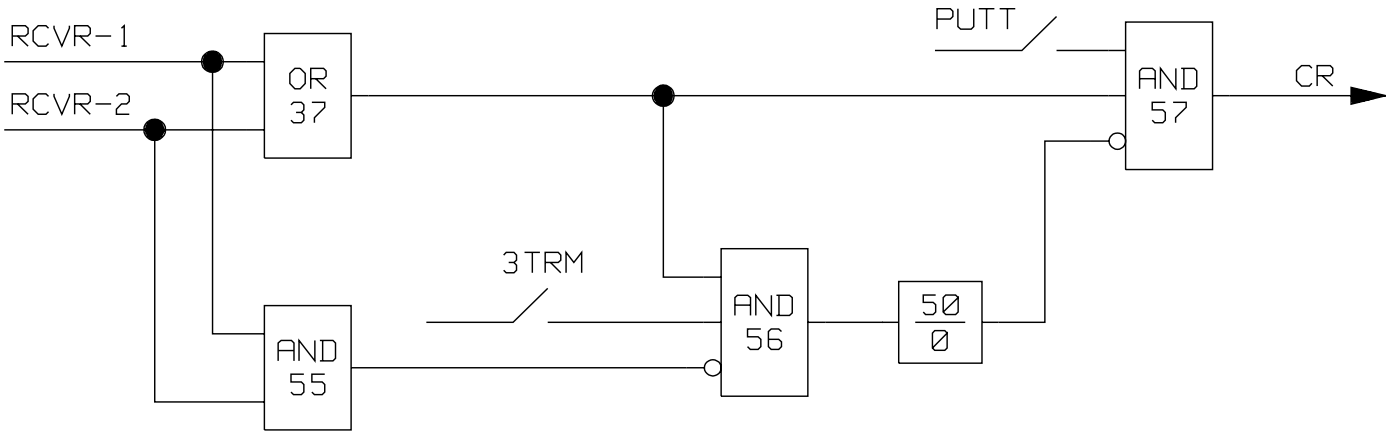


Sub 1
9654A29

Figure 3-28 Unequal Pole Closing on Fault.

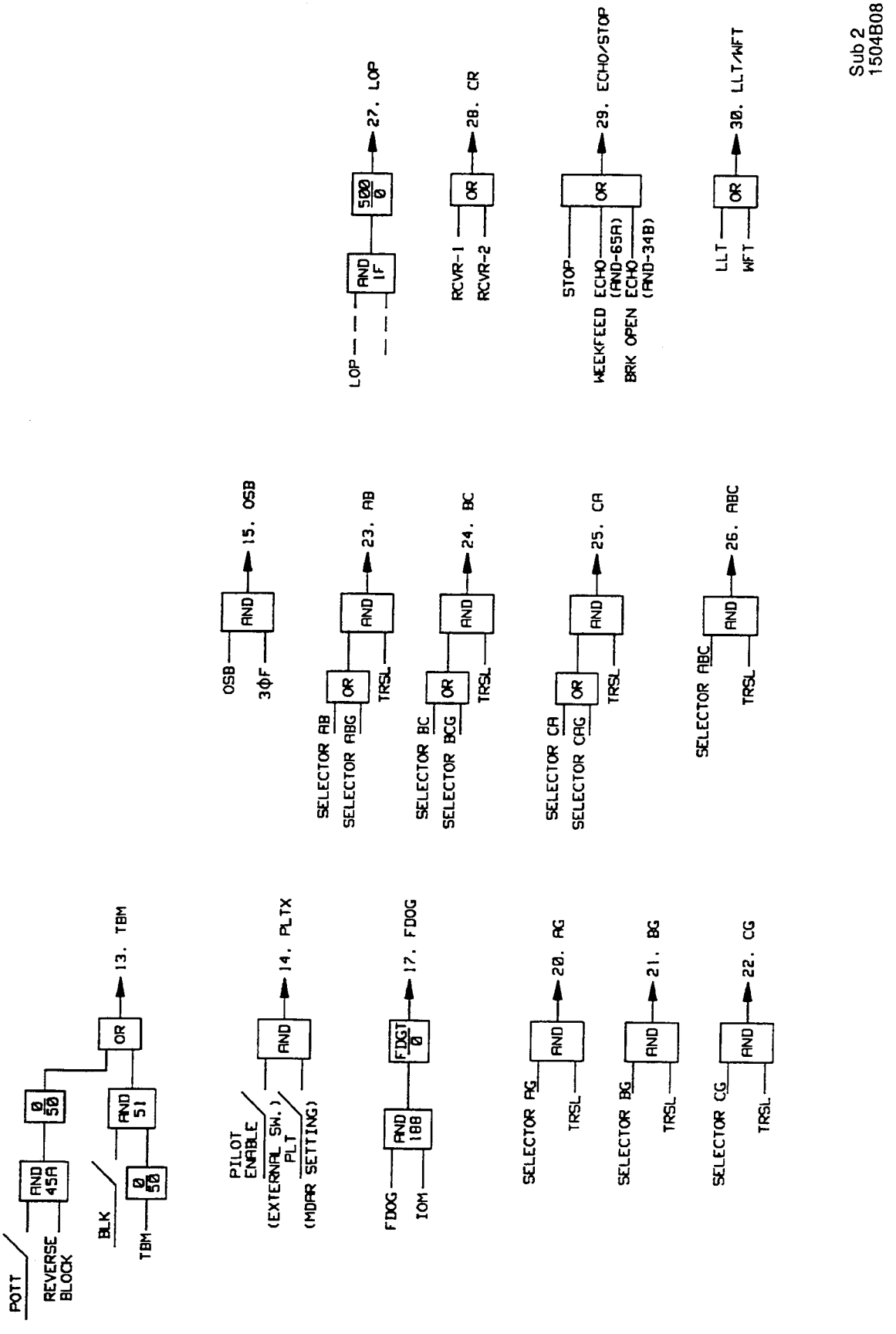
Sub 1
9654A30

Figure 3-29 Additional Logic for POTT/Unblocking Schemes on 3-Terminal Line Application.



Sub 1
9654A31

Figure 3-30 Additional Logic for PUTT Scheme on 3-Terminal Line Application.

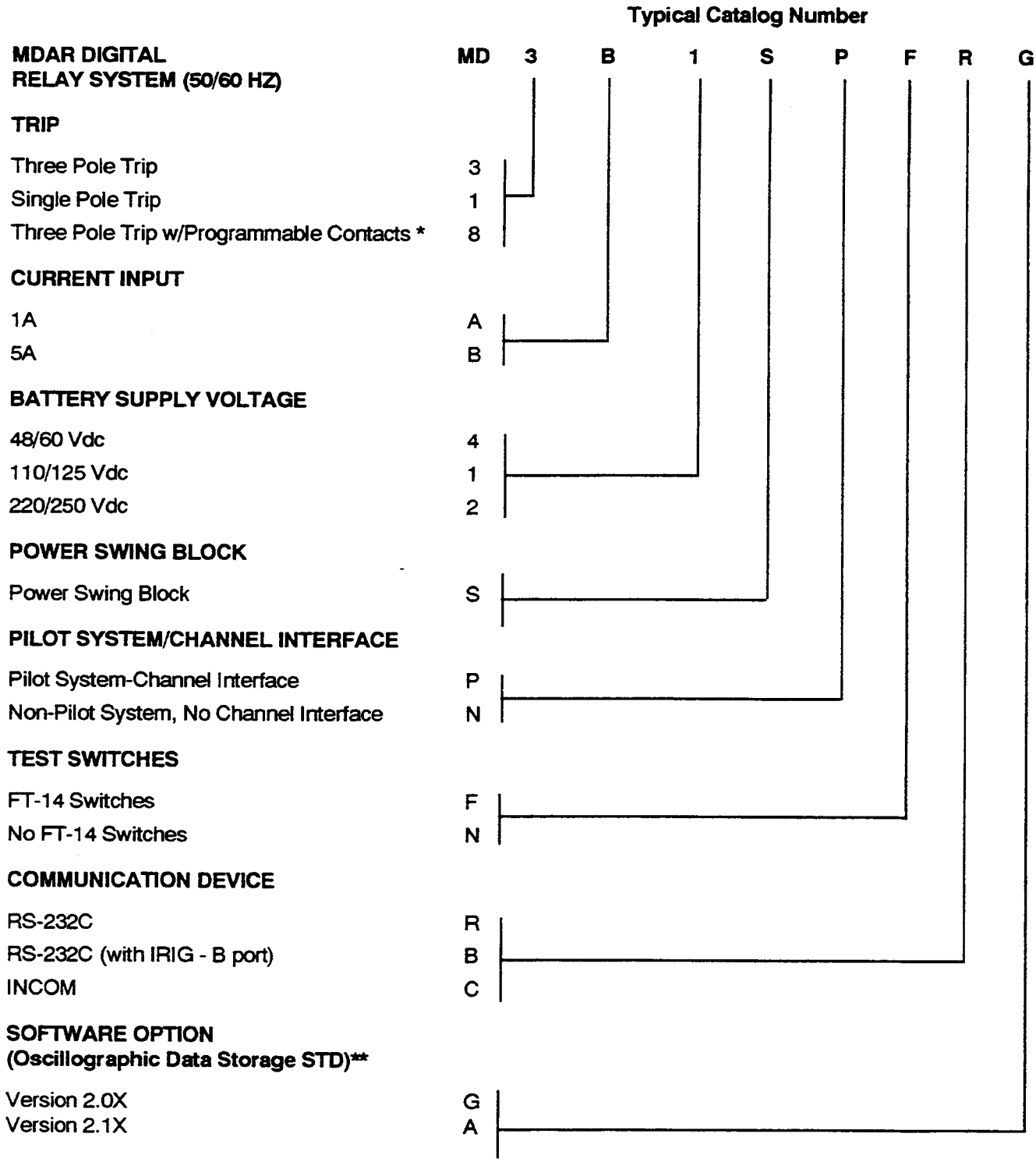


Sub 2
1504B08

Figure 3-33. Composite Signal For Programmable Output Contacts

TABLE 3-1

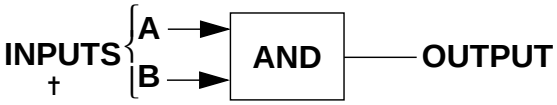
MDAR CATALOG NUMBERS



* Available in 2.1X Version only

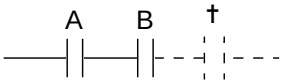
** The optional Oscillographic and Recording software (OSCAR) can be ordered separtely, catalog number SWOSC01

AND



INPUTS		OUTPUT
A	B	
0	0	0
0	I	0
I	0	0
I	I	I

ELECTROMECHANICAL CONTACT EQUIVALENT



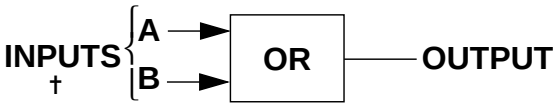
SIGNAL ON ALL INPUTS REQUIRED TO PROVIDE AN OUTPUT

Notes: I – Active state of a signal (may be defined as positive or negative voltage or current)

0 – Inactive state of a signal (reference)

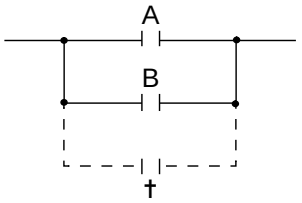
† – Can have more than two (2) inputs

INCLUSIVE OR



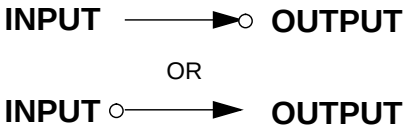
INPUTS		OUTPUT
A	B	
0	0	0
0	I	I
I	0	I
I	I	I

ELECTROMECHANICAL CONTACT EQUIVALENT



SIGNAL INPUT WILL PRODUCE AN OUTPUT
ALL INPUTS PRODUCE AN OUTPUT

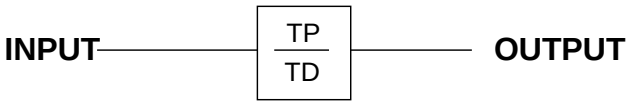
NEGATION (NOT)



INPUTS	OUTPUT
0	I
I	0

ABSENCE OF INPUT SIGNAL PRODUCES OUTPUT

TIMERS



Input changes to Active State “1” - Output changes to Active State After Time Delay “On Pickup” (TP)

Input Changes to Inactive State “0” (Only After Having Been Active) - Output Changes to Inactive State After Time Delay “On Dropout”

Figure 3-34. Logic Drawing Symbols

TABLE 3-1

MDAR CATALOG NUMBERS

Typical Catalog Number

		MD	3	B	1	S	P	F	R	G
MDAR DIGITAL RELAY SYSTEM (50/60 HZ)										
TRIP										
Three Pole Trip		3								
Single Pole Trip		1								
Three Pole Trip w/Programmable Contacts *		8								
CURRENT INPUT										
1A		A								
5A		B								
BATTERY SUPPLY VOLTAGE										
48/60 Vdc		4								
110/125 Vdc		1								
220/250 Vdc		2								
POWER SWING BLOCK										
Power Swing Block		S								
PILOT SYSTEM/CHANNEL INTERFACE										
Pilot System-Channel Interface		P								
Non-Pilot System, No Channel Interface		N								
TEST SWITCHES										
FT-14 Switches		F								
No FT-14 Switches		N								
COMMUNICATION DEVICE										
RS-232C		R								
RS-232C (with IRIG - B port)		B								
INCOM		C								
SOFTWARE OPTION (Oscillographic Data Storage STD)**										
Version 2.0X		G								
Version 2.1X		A								

* Available in 2.1X Version only

** The optional Oscillographic and Recording software (OSCAR) can be ordered separately, catalog number SWOSC01

TABLE 3-2

MDAR ACCESSORIES

1. FT-14 TEST PLUG
   - Right-Side 1355D32G01
   - Left-Side 1355D32G02

2. TEST FIXTURE AND EXTENDER BOARD
   - Inner Chassis Test Fixture (5 Amp) 2409F39G01
   - Inner Chassis Test Fixture (1 Amp) 2409F39G02
   - External Board Assembly 1609C55G01

TABLE 3-3

SINGLE-POLE-TRIP OPERATING MODES

"TTYP" SET AT POSITION	TRIP MODE	RECLOSING INITIATE
OFF	3PT on all faults	No reclosing
1PR	3PT on all faults	RI2 on ϕG faults only
2PR	3PT on all faults	RI2 on ϕG/$\phi\phi$/$\phi\phi$G faults
3PR	3PT on all faults	RI2 on all faults
SPR	SPT on ϕG faults 3PT on others	RI1 on ϕG faults only no reclosing on others
SR3R	SPT on ϕG faults 3PT on others	RI1 on ϕG faults RI2 on others

TABLE 3-4

MDAR PROGRAMMABLE OUTPUT CONTACTS

		Description	Value
	10.	Z1P trip output	Z1P
	11.	Z1G trip output	Z1G
	12.	Z2P trip output	Z2P
	13.	Z2G trip output	Z2G
	14.	Z3P trip output	Z3P
	15.	Z3G trip output	Z3G
	16.	PLTP trip output	PLTP
	17.	PLTG trip output	PLTG
	18.	High set phase trip output	ITP
	19.	High set ground trip output	ITG
	20.	GB trip output	GB
	21.	Close-into-fault trip output	CIFT
●	22.	TBM signal output (BLK/POTT)	TBM
●	23.	Pilot in service	PLTX
●	24.	OSB pickup	OSB
	25.	Carrier send output	SEND
●	26.	FDOG/IOM/FDGT output	FDOG
	27.	Inner blinder 21BI pickup	21BI
	28.	IOS without timer	IOS
●	29.	Phase selector AG	AG
●	30.	Phase selector BG	BG
●	31.	Phase selector CG	CG
●	32.	Phase selector AB of ABG	AB
●	33.	Phase selector BC or BCG	BC
●	34.	Phase selector CA or CAG	CA
●	35.	Phase selector ABC with TRSL	ABC
●	36.	LOP with delay pickup/without delay dropout	LOP
●	37.	RCVR-1 or RCVR-2	CR
●	38.	POTT scheme — ECHO (either weakfeed or open breaker key) BLK scheme — STOP	ECHO/STOP
●	39.	LLT or WFT	LLT/WFT

● ***Refer to Figure 3-33 for the signals and logics.***

Section 4. INSTALLATION, OPERATION AND MAINTENANCE

WARNING

Check jumper #3 on the Microprocessor module for phase rotation ABC or ACB. Remove jumper#3 for system ABC rotation. Refer to section 1.8 for ACB system.

4.1 SEPARATING THE INNER AND OUTERCHASSIS

It is recommended that the user of this equipment become acquainted with the information in these instructions before energizing the MDAR and associated assemblies. Failure to observe this precaution may result in damage to the equipment.

All integrated circuits used on the modules are sensitive to and can be damaged by the discharge of static electricity. Electrostatic discharge precautions should be observed when operating or testing the MDAR.

CAUTION

Use the following procedure when separating the inner chassis from the outer chassis; failure to observe this precaution can cause personal injury, undesired tripping of outputs and component damage.

a. Unscrew the front panel screw.

b. If the MDAR does not have FT-14 switches, but has a power switch on the front panel, turn “OFF” the power switch before sliding out the inner chassis.

c. If the MDAR has FT-14 switches:

1) Remove the FT-14 covers (one on each side of the MDAR).

2) Open all FT-14 switches.

WARNING

Do Not Touch the outer contacts of any FT-14 switch; they may be energized.

3) Slide out the inner chassis.

4) Close all FT-14 switches.

5) Replace the FT-14 covers.

d. Reverse procedures above when replacing the inner chassis into the outer chassis.

4.2 TEST PLUGS AND FT-14 SWITCHES

Test Plugs are available as accessories (**see Table 3-2**); they are inserted into the FT-14 switches for the purpose of System Function Tests. When the Test Plugs are inserted, the FT switch #13 (BP) and #14 (BN) must remain closed.

4.3 EXTERNAL WIRING

All external electrical connections pass through the Backplate (**Figure 4-1**) on the outer chassis. If the MDAR is used without the FT-14 switch, six 14-terminal connectors on the Backplate (TB1 through TB6) are used. If the FT-14 switch (option) is included, using the two peripheral areas of the MDAR cabinet, then only four of the 14-terminal connectors (TB2 through TB5) are used. Three DIN connectors (J11, J12, J13) allow for the removal of the outer chassis (Backplane module) from the inner chassis (Interconnect module).

Electrical inputs to the Backplane module, which are routed either directly through the Backplate or through the FT-14 switch to the Backplate, include (**Figure 4-1**):

- V_A, V_B, V_C and V_N
- I_A/I_{AR}, I_B/I_{BR}, I_C/I_{CR}, and I_P/I_N
- BP (48, 125 or 250 Vdc) and BN (negative)

Analog input circuitry consists of four current transformers (I_A, I_B, I_C, and I_N), three voltage transformers, (V_A, V_B and V_C), and low-pass filters. The seven

transformers are located on the Backplane PC Board (see **Appendix A**). The primary winding of all seven transformers are directly-connected to the input terminal TB6/1 through 12 (see **Functional Block Diagram, Appendix J**); the secondary windings are connected through the Interconnect module to the Filter module.

As shown in Figures 4-1 and 4-2, dry contact outputs for breaker failure initiation (BFI), reclosing initiation (RI), reclosing block (RB), failure alarm (AL1), trip alarm (AL2), SEND and STOP are located on the Backplane PC Board. Optical isolators are for Pilot Enable, External Reset, Receiver #1 and #2, 52a, 52b, SBP (89b) and studs for chassis ground (GND) and location for the Communication Interface are also shown.

As shown in Figure 4-3, the power system ac quantities (V_a, V_b, V_c, V_n, I_a, I_b, I_c and I_n), as well as the dc source are connected to the left side FT-14 switch (front view). All the trip contact outputs are connected to the right-side FT-14 switch (front view). Switches 13 and 14 on FT-14 may be used for disabling the Breaker Failure Initiation/Reclosing Initiation (BFI/RI) control logic. (**See also external connections, Block Diagram, Appendix J**.)

The INCOM® or RS232C PONI (Product Operated Network Interface) communication box is mounted through the Backplate of the outer chassis and connected to the Backplane module, and remote settings (**see section 4.7**).

4.4 MDAR FRONT PANEL DISPLAY

The front panel display consists of a vacuum fluorescent display, seven LED indicators, seven pushbutton switches, and five test points (**as shown in Figure 1-1**).

4.4.1 Vacuum Fluorescent Display

The vacuum fluorescent display (blue color) contains four alphanumeric characters for both the function field and the value field. All the letters or numbers are fourteen segment form (7.88mm x 13mm in size).

A software display saver is built in. The MDAR display will be on only for 5 minutes after turning on the dc power supply or depressing any one of the front panel pushbuttons or detecting any fault on the line.

4.4.2 LED Indicators

There are seven LED indicators on the front panel display:

- 1 “relay-in-service” indicator
- 1 “value accepted” indicator
- 5 display-select indicators

When the “Relay-in-Service” LED illuminates, the MDAR Relay is in service, there is dc power to the relay and the relay has passed the self-check and self-test. The LED is turned “OFF” if the Relay-in-service relay has at least one of the internal failures shown in the “Test” mode, and the trip will be blocked.

The “Value Accepted” LED flashes only once, to indicate that a value has been entered successfully.

The five indicators used for the display selection are:

- Settings
- Volts/Amps/Angle
- Last Fault
- Previous Fault
- Test

One of these indicators is always illuminated, indicating the mode selected. The display will be blocked momentarily every minute for the purpose of self-check; this will not affect the relay protection function.

4.4.3 Pushbutton Switches

The front panel contains seven pushbutton switches:

- Display Select
- Reset Targets
- Function Raise
- Function Lower
- Value Raise
- Value Lower
- Enter (recessed for security purposes)

The “Display Select” pushbutton is used to select one of the five display modes, which is indicated when the proper LED illuminates. When a fault is detected, the “Last Fault” flashes once per second. If two faults are recorded, the “Last Fault” flashes twice per second, and the prior fault will be moved from “Last Fault” to “Previous Fault”. The new fault data will be stored in the “Last Fault” register. By depressing the “Reset Targets” pushbutton, the flashing LED indicators are cleared, and the LED will revert back to the Metering mode. The information in the “Previous Fault” and “Last Fault” will not be reset from the front panel pushbutton switch, but will be re-

set from External Reset (TB5/5 and TB5/6) and the remote reset through the Communication Interface.

The “Function Raise” and “Function Lower” pushbuttons are used to scroll through the information for the selected display mode. The “Value Raise” and “Value Lower” pushbuttons are used to scroll through the different values available for each of the five functions. The “Enter” pushbutton is used to enter (in memory) a new value for settings.

If the display is in “sleep” mode (no readout), by depressing any one of the pushbuttons will resume the illumination of the vacuum fluorescent display.

4.4.4 Test Points

Five test points are provided to check the dc power supply. Refer to these test points on the front panel display:

- -24V
- + 5V
- -12V
- +12V
- Common

Each measurement is taken by inserting one dc probe (voltmeter) into Common, and the other dc probe at the voltage being measured.

4.5 FRONT PANEL OPERATION

The front (operator) panel provides a convenient means of checking or changing settings, and for checking relay unit operations after a fault. Information on fault location, trip types, phase, operating units, and breakers which tripped become available by using the pushbuttons to step through the information. Targets (fault data) from the last two faults are retained, even if the relay is deenergized. The operator is notified that targets are available by a red flashing LED on the front panel; in addition, alarm 2 output-relay contacts are provided for the external annunciators.

The operator can identify nonfault voltage, current and phase angle on the front panel display. Settings can be checked easily, however, any change to the settings requires the use of the pushbuttons. When relay is in the normal operating mode, it is good practice to set the LED on the Volts/Amps/Angle mode.

4.5.1 Settings Mode

In order to determine the MDAR settings that have been entered into the system, continually depress the “DISPLAY SELECT” pushbutton until the “SETTINGS” LED is illuminated. Then depress the “FUNCTION RAISE” or “FUNCTION LOWER” pushbutton, in order to scroll through the MDAR SETTINGS functions (**see Table 4-1**). For each settings function displayed, depress the “VALUE RAISE” or “VALUE LOWER” pushbutton in order to scroll through the MDAR values available for the particular function. (Each value that appears, as each different function appears in the function field, is considered to be the “current value” used for that particular function.)

In order to change the “current value” of a particular settings function, “RAISE” or “LOWER” the FUNCTION field until the desired function appears (e.g., “RP”). Then “RAISE” or “LOWER” the values in the VALUE field until the desired value appears. If the “ENTER” pushbutton (recessed for security purposes) is depressed, the value which appears in the VALUE field will replace the “current value” in memory; but only if the “VALUE ACCEPTED” LED flashes once to indicate that the value has been successfully entered into the system.

For reasons of security, a plastic screw is used to cover the ENTER pushbutton. A wire can be used to lock the plastic screw and to prevent any unauthorized personnel from changing the settings.

4.5.2 Metering (Volts/Amps/Angle) Mode

When the Volts/Amps/Angle LED is selected by the “Display Select” pushbutton, the phase A, B, C voltages, currents and phase angles are available for on-line display during normal operation. All measured values can be shown by scrolling the “Raise” or “Lower” pushbutton in the FUNCTION field. The values on the display are dependent on the settings of RP (read primary); RP= YES for the primary side values and RP = NO for the secondary values. Conditions such as loss-of-potential, loss-of-current and out-of-step blocking can also be monitored. The function names and values are shown in **Table 4-2.**

NOTE: All displayed Phase Angles use V_A as reference.

The phase rotation of ABC or ACB is also displayed on the metering mode depends on the setting of JMP3 position on processor module.

4.5.3 Target (Last and Previous Fault) Mode

The MDAR system saves the latest 16 faults records. The “LAST FAULT” information is of the most recent fault, the “PREVIOUS FAULT” information is of the fault prior to the “LAST FAULT”. These displays contain the target information along with the

"frozen" data at the time of trip. The "LAST FAULT" register shows one or two records stored by flashing the LED once or twice per second, respectively. These records can be deleted by External Reset voltage TB/5 (+) and TB5/6 (-) or through a remote communication interface. The front panel (RESET) pushbutton allows the user to reset the flashing LED to Metering position only. It will not erase the fault in formation.

Different types of faults with related descriptions are shown in **Table 4-3**. As soon as a fault event is detected, the most recent two sets of target data are available for display. If the FDAT is set at "TRIP", the "Last Fault" is the data associated with the most recent trip event. The "Previous Fault" contains the data from the prior trip event. If a single fault occurs, the "Last Fault" LED flashes. If a reclosing is applied and the system trips, the original "LAST FAULT" information will be transferred to the "Previous Fault" memory. The latest trip information will be stored in the "Last Fault" memory, and its LED flashes twice per second. If FDAT is set at Z2TR, two events (Zone-2 pickup or trip) will be stored. If FDAT is set at Z2/Z3, the two events will be either Zone-2 pickup or Zone-3 pickup or any type of trip. The same description applies to a remote communication which can store up to 16 events.

4.5.4 Test Mode (Self-Check Routine)

The software of the MDAR relay contains several self-check routines (**see Section 1.6**). When the "Test" mode is selected by the "Display Select" pushbutton, the failure modes (represented by their corresponding bits) are shown in the VALUE field, as follows:

- Bit 0 External RAM Failure
- Bit 1 EEPROM Warning
- Bit 2 ROM Failure
- Bit 3 EEPROM Failure (NON-Volatile memory)
- Bit 4 Analog Input Circuit Failure
- Bit 5 Microprocessor Failure
- Bit 6 Setting Discrepancy

Data types are as follows:

- bit
- byte = 8 bits
- word = 16 bits
- longword = 32 bits

All bits are expressed in HEX byte form. For example, if the display shows "Test 1B", whose binary representation is 00011011, this means that the relay failed the self-check in the area of External RAM (bit 0), EEPROM (one-out-of-three failure, bit 1), (two-out-of-three failure, bit 3) and Analog Input Circuit (bit 4). Normally, the test mode should show "Test 0", meaning that the relay has passed the self-check routines.

Bit 6 is for the setting discrepancy detection. If the ordering information calls for single-pole trip option and the jumper #2 on the Microprocessor module is on position "1-2" which is for the Programmable output contacts, the MDAR will give the error of "TEST 40".

⚠ CAUTION

When the selector is in TEST mode, scroll the function field by the Raise pushbutton. The Value field display shows RS1 (Carrier Receiver #1), RS2 (Carrier Receiver #2), RS1, 2 (Carrier Receiver #1 and #2), and "TK" (Carrier Send) for the use of MDAR functional test. Refer to the Pilot Acceptance Test (Appendix H, Section 1.1.13) for more detailed information. If jumper (JP5) on the microprocessor module is IN, the following ten functions will be shown:

- TRIP
- BFI
- RI1
- RI2
- RB
- AL1
- AL2
- GS
- SEND
- STOP

All of these contact outputs can be tested by pressing the "ENTER" pushbutton. (**see Appendix I, Section 1.13).**

4.6 JUMPER CONTROLS

The following jumpers are set at the factory; the customer normally does not need to move the jumpers. **Refer to Table 4-4** for the recommended jumper positions.

4.6.1 Backplane Module

An external jumper should be wired to the right side FT switch #13 (term. #2) and #14 (term #4). **See Figure 4-3**.

When FT switch #13 or #14 is opened, the BFI and RI output relays are disabled to prevent BFI and RI contact closures during system function test.

4.6.2 Interconnect Module

The factory sets jumpers (JMP1 through JMP6 and JMP13) for 48 Vdc or 125 Vdc input source.

JMP7 & 9 are used for Stub Bus Protection (SBP). If SBP is not used, move JMP7 & 9 to 8 & 10 position for the second set of AL2-2 use.

If the customer intends to use a voltage other than 48 Vdc or 125 Vdc, see Interconnect Module Schematic, Appendix B.

4.6.3 Microprocessor Module

The following jumpers are normally set during factory calibration:

- JMP1, JMP8, JMP9 — for EEPROM and RAM circuitries, and are normally set to position 1-2.
- JMP2 — normally set to position 1-2 for three pole trip or programmable output contact logic. Set position 2-3 for single-pole trip logic only.
- JMP3 — Phase rotation; “OUT” for ABC, “IN” for ACB
- JMP4 — set to “IN” for trip contact with dropout time delay.
- JMP5 — set to “IN” for output contact tests. Normally, set to “OUT”.
- JMP6 — normally set to “OUT” position; set to “IN” when making A/D converter calibration.
- JMP10, JMP11, JMP12 — Not used (or spare jumpers)

NOTE: Should the customer need to gain access to any of the jumpers (above), see Section 4.10, and Appendix E.

4.6.4 Power Supply Module

- JMP1 Carrier Stop — Position 1-2 for NO contact and 2-3 for NC contact output.
- JMP2 Carrier SEND — Position 1-2 for NO contact and 2-3 for NC contact output.

4.6.5 Programmable Output Contact Module

- JMP1 — Selection for NO or NC output contact of OC5.
- JMP2 — Selection for NO or NC output contact of OC6.
- JMP3 — Selection for NO or NC output contact of OC7.
- JMP4 — Selection for NO or NC output contact of OC8.

4.7 COMMUNICATION INTERFACE

Two options are available for interfacing between MDAR and a variety of local and remote communication devices.

- RS232C - for single point computer communication
- INCOM®/PONI[1] - for local network communication

An IBM® AT or XT[2] compatible computer, with software provided (WRELCOM®), can be used to monitor the settings, 16 fault data, 16 intermediate data, and metering information. For a remote setting, SETR should be set to “YES”; then the settings can be changed (remotely) with a user-defined password. If a user loses his assigned password, a new password can be installed by turning the MDAR relay’s dc power supply “OFF” and then “ON”. MDAR allows a change of password within the next 15 minutes, by using a default “PASSWORD”.

When in the remote mode, the computer can disable the local setting by showing SET = REM (in the Metering mode). Then, the setting cannot be changed locally. In this situation, the only way to change a setting locally would be to turn the dc power “OFF” and then “ON”. The computer will allow for a local setting change within 15 minutes.

4.8 SIXTEEN FAULT TARGET DATA

The MDAR saves the latest 16 fault records, but only the latest two fault records can be accessed from the front panel. For complete 16 fault data, one of the communication interface devices are necessary.

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1 INCOM is the registered trademark of the Westinghouse Electric Corporation, Inc., which stands for INtegrated COMmunications. The “PONI” acronym stands for Product Operated Network Interface.

2 IBM is the registered trademark of International Business Machines Company, Inc.

The activation of fault data storage is controlled by setting FDAT. (**Refer to Section 3.4.19** for detailed information.) The 16 intermediate fault targets are a standard feature. The activation of data storage is based on the setting of the optional OSC (**see next section**).

4.9 OSCILLOGRAPHIC DATA (Standard) (Optional Graphic Feature)

Sixteen sets of oscillographic data are stored in MDAR. Each set includes seven analog traces (V_a, V_b, V_c, I_a, I_b, I_c and I_n), with one cycle pre-fault and 7-cycle fault information, and 20 sets of digital data based on 8 samples per cycle.

The oscillographic data (OSC) collection can be set for TRIP, Z2TR, Z2/Z3, and $\Delta V \Delta I$. For setting of OSC = TRIP, data are collected for the trip events. The data collection is started from $\Delta V \Delta I$ if the trip occurs within 7 cycles. For OSC = Z2TR, the data collection is triggered by Zone-2 pickup or any types of trip. For OSC = Z2/Z3, the collection is triggered by either Zone-2 or Zone-3 pickup (including the Zone-3 reverse setting) or TRIP. For OSC = $\Delta V \Delta I$, the data collection is caused by any line disturbance, e.g., a sudden phase current change (by 1 amp) or a ground current change (by 0.5 Amp), or a voltage change (ΔV) greater than 7Vdc.

NOTE: Setting at $\Delta V \Delta I$ is not recommended because a lot of meaningless data will be stored, such as breaker opening or closing, etc.

4.10 PROGRAMMABLE CONTACT OUTPUTS (Optional Feature)

The optional programmable output contact module consists of 8 relays, 4 with heavy duty NO contacts (OC1 to OC4) and 4 with standard contacts (OC5 to OC8) with jumper selection for NO or NC outputs. Contacts OC4 and OC8 provide timers for delay pickup and/or delay dropout. The ranges of timers are 0 to 5 seconds in 0.01 seconds steps with an error of 1 cycle. Every Contact (OC1 to OC8) can be programmed independently based on one or all of the 30 pre-assigned signals with AND/OR logic combination. These 30 signals are listed in **Table 3-4** and **Figure 3-33**. All 8 output settings can only be performed through remote WRELCOM™ communication. An example of this programmable contact output WRELCOM™ screen is shown in **Table 4-5**.

Selecting a function for an output contact is made by pressing the INSERT key with the cursor positioned at the crossing of the desired function and contact number.

The DELETE key can be used to de-select a previously selected function.

If a contact is to be controlled by several functions, the same procedure applies for each function, without forgetting the combining operator OR or AND. To input a pickup or dropout time delay (contact #4 or #8 only), press ENTER with the cursor positioned on the appropriate time delay. Press ENTER again to accept the desired time delay.

4.11 ROUTINE VISUAL INSPECTION

With the exception of Routine Visual Inspection, the MDAR relay assembly should be maintenance-free for one year. A program of Routine Visual Inspection should include:

- Condition of cabinet or other housing
- Tightness of mounting hardware and fuses
- Proper seating of plug-in relays and subassemblies
- Condition of external wiring
- Appearance of printed circuit boards and components
- Signs of overheating in equipment

4.12 ACCEPTANCE TESTING

The customer should perform the MDAR Acceptance Tests (**see Appendix I**) on receipt of shipment.

4.13 NORMAL PRECAUTIONS

Troubleshooting is not recommended due to the sophistication of the Microprocessor unit.

CAUTION

With the exception of checking to insure proper mating of connectors, or setting jumpers, the following procedures are normally not recommended. (If there is a problem with the MDAR, it should be returned to the factory. See *PREFACE.)*

4.14 DISASSEMBLY PROCEDURES

a. Remove the inner chassis from the outer chassis, by unscrewing the center lockscrew (on the front panel), and unsnapping the two covers from the (optional) FT-14 switches, if the FT-14 switches are a part of the MDAR system.

NOTE: The inner-chassis (sub-assembly) slides in and out of the outer chassis from the front. Mating connectors inside the case eliminate the need to disconnect external wiring when the inner chassis is removed.

b. Remove the (optional) FT-14 switches, mounted by two screws on the side walls.

c. Remove the front panel (with the Display module) from the inner chassis, by unscrewing four screws behind the front panel.

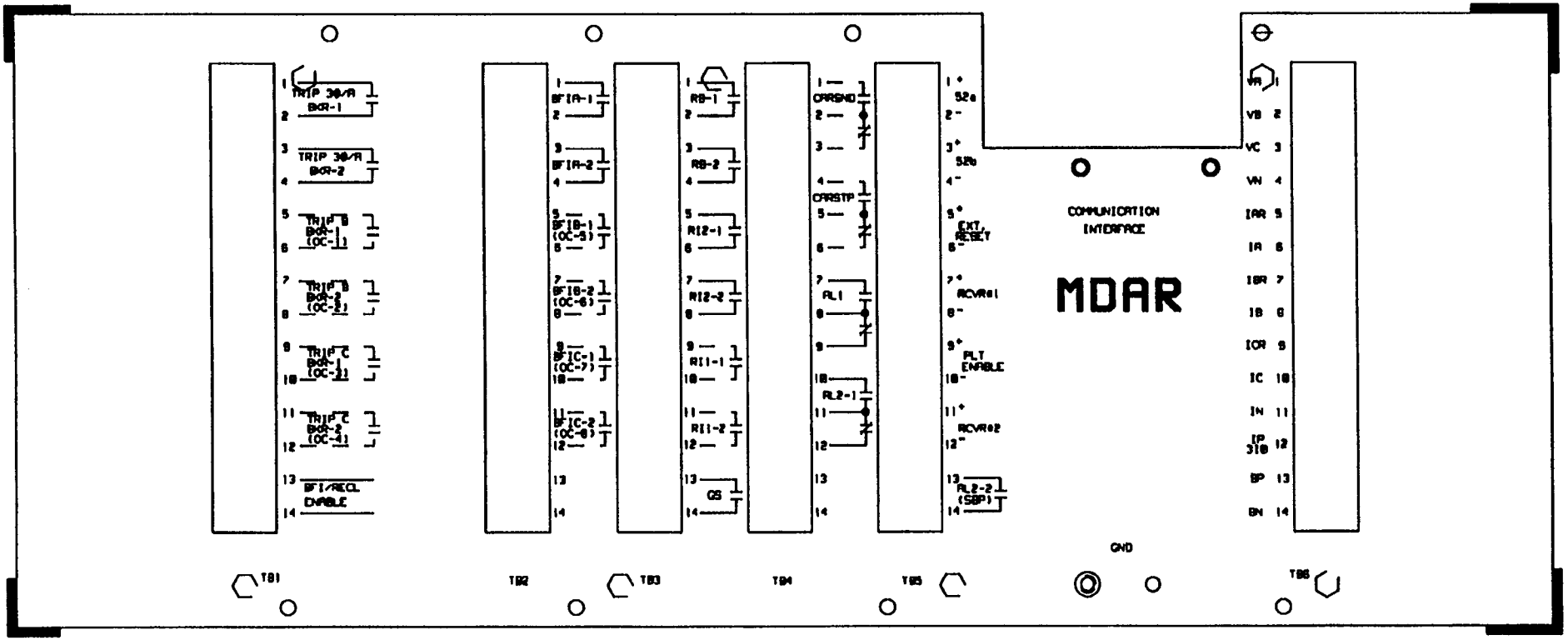
d. Remove the Microprocessor module, by loosening six mounting screws, and unplugging the module from the Interconnect module.

e. Remove the Option (module), if the option module is part of the MDAR system, by unscrewing 2 mounting screws from the center support bar, and unplugging the Option module from the Interconnect module.

f. Remove the Power Supply and Filter modules, by first removing the Microprocessor module and the support cross bar.

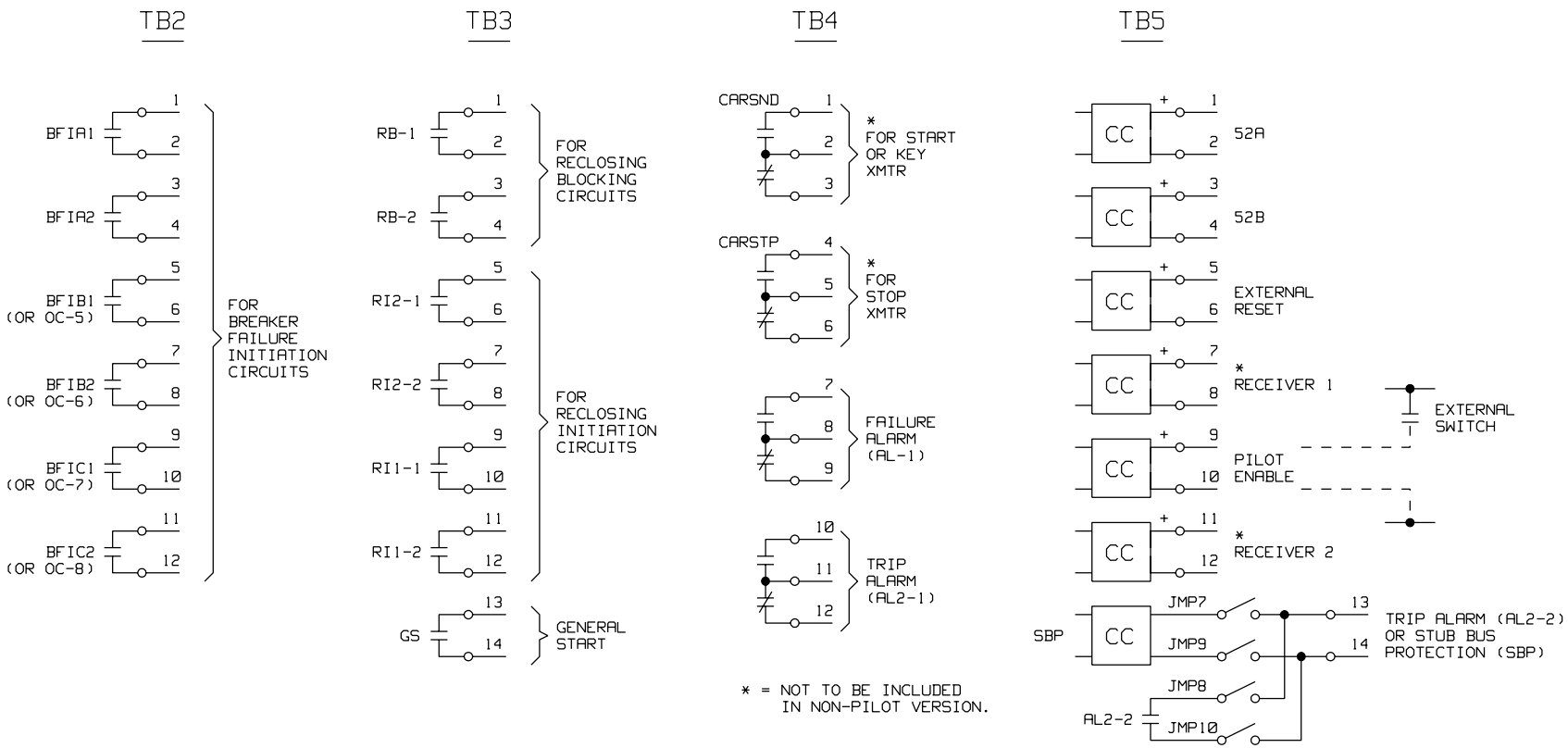
g. Remove the Backplate, by unscrewing the mounting hardware from the rear of the Backplate.

h. Gain access to the Backplane and Transformer modules, by removing the Backplate.



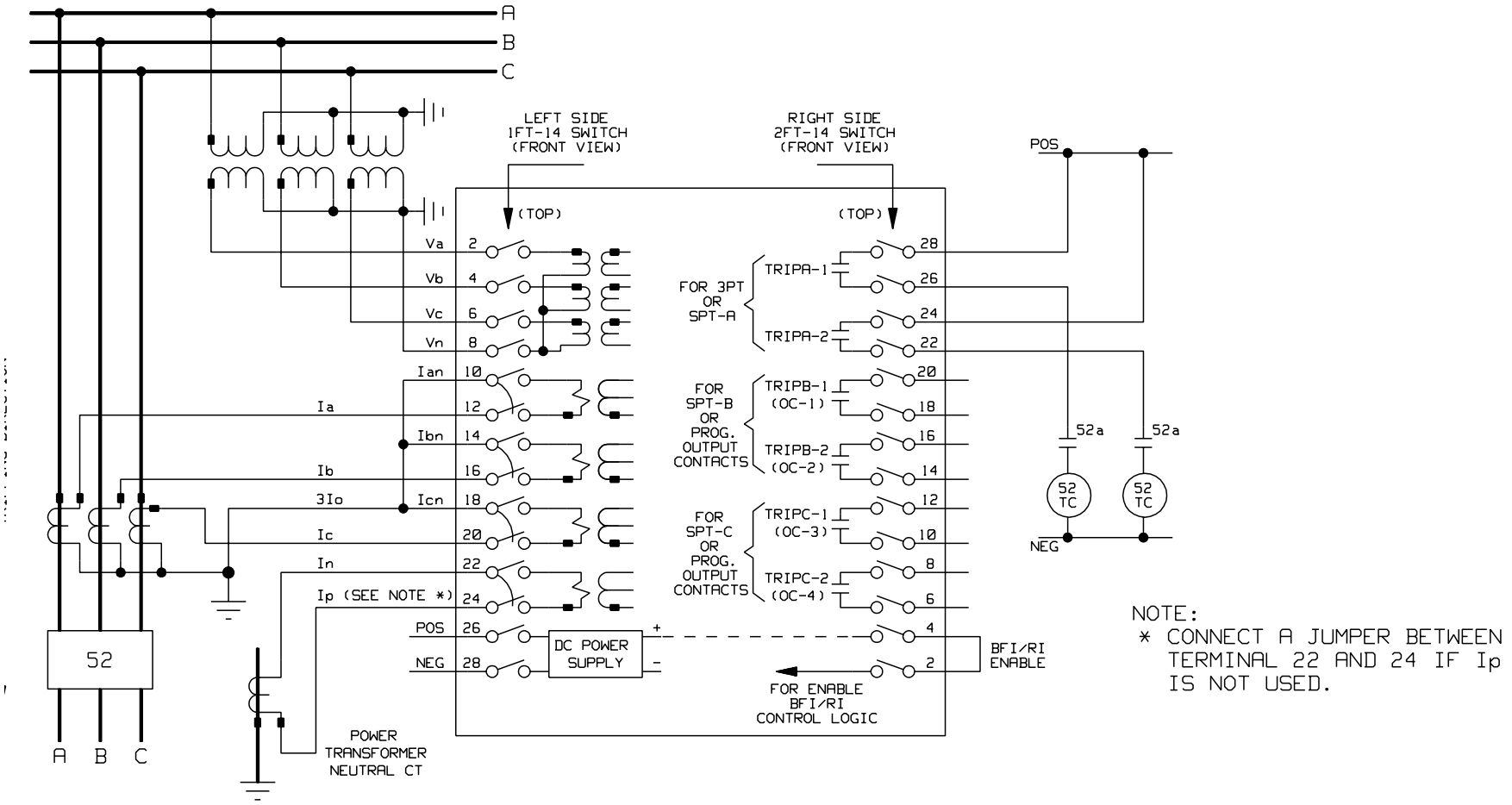
Sub 6
1354D22
Sheet 4 of 5

Figure 4-1 MDAR Backplate.



Sub 1
1611C78

Figure 4-2 MDAR Backplane PC Board Terminals



Sub 3
1502B21

Figure 4-3 MDAR Systems External Connection.

TABLE 4-1. SETTING DISPLAY (SHEET 1 OF 3)

Information/Settings	Displayed at Function Field	Value Field (using 5 A ct and 60 Hz) (SEE NOTE ON SHEET 3)
Software version	VERS	numerical (0,1)
Oscillographic data initiation	OSC *	TRIP/Z2TR/Z2Z3/ΔVΔI
Fault data initiation	FDAT	TRIP/Z2TR/Z2Z3
ct ratio	CTR	30-5000 (5)
PT ratio	VTR	100-7000 (5)
Rated freq.	FREQ	60, 50
ct secondary rating	CTYP	5 or 1
Enable/disable readouts in primary I & V values	RP	YES/NO
Reactance for fault location (ohms per unit distance)	XPUD	0.300-1.500, in 0.001/DTYP
Fault location, displayed in km or miles	DTYP	KM or MI (miles)
Reclosing mode	TTYP	
1. 3PT on all faults, no RI		OFF
2. 3PT on all faults, with 3RI on ϕGF		1PR
3. 3PT on all faults, with 3RI on ϕGF/2ϕF		2PR
4. 3PT on all faults, w/3RI		3PR
5. SPT on ϕGF with SRI 3PT on MϕF without RI		SPR
6. SPT on ϕGF with SRI 3PT on MϕF with 3RI		SR3R
Single phasing limit timer	62T *	0.300-5000, in 0.050 sec. steps
RI on Z1T	Z1RI	YES/NO
RI on Z2T	Z2RI	YES/NO
RI on Z3T	Z3RI	YES/NO
Breaker Failure Reclose block	BFRB	YES/NO
Pilot logic control	PLT	YES/NO
Pilot system selection:	STYP	
1. Non-Pilot, 3-zone distance		3ZNP
2. Zone-1 extension		Z1E
3. Permissive overreach transfer trip or unblocking		POTT
4. Permissive underreach transfer trip		PUTT
5. Blocking		BLK
Forward Direction Ground Timer	FDGT	BLK, 0 to 15 cycles in 1cycle steps
Weakfeed Enable	WFEN	YES/NO
3-Terminal Line Application	3TRM	YES/NO
Blocking system channel		
Coordination timer	BLKT	0-98, in 2 ms steps
Pilot phase setting	PLTP	OUT, 0.01-50.00 in 0.01 Ω steps
Pilot ground setting	PLTG	OUT, 0.01-50.00 in 0.01 Ω steps

Optional

TABLE 4-1. SETTING DISPLAY (SHEET 2 OF 3)

Information/Settings	Displayed at Function Field	Value Field (using 5 A ct and 60 Hz) (SEE NOTE ON SHEET 3)
Zone-1 phase unit	Z1P	OUT, 0.01-50.00 in 0.01 Ω steps
Zone-1 ground unit	Z1G	OUT, 0.01-50.00 in 0.01 Ω steps
Zone-1 delay trip timer	T1	YES/NO, 2 cycles if YES
Zone-2 phase unit	Z2P	OUT, 0.01-50.00 in 0.01 Ω steps
Zone-2 phase timer	T2P	BLK, 0.10-2.99, in 0.01 sec. steps
Zone-2 ground unit	Z2G	OUT, 0.01-50.00 in 0.01 Ω steps
Zone-2 ground timer	T2G	BLK, 0.10-2.99, in 0.01 sec. steps
Zone-3 phase unit	Z3P	OUT, 0.10-50.00 in 0.01 Ω steps
Zone-3 phase timer	T3P	BLK, 0.10-9.99 in 0.01 sec. steps
Zone-3 ground unit	Z3G	BLK, 0.01-50, 0.01 Ω steps
Zone-3 ground timer	T3G	BLK, 0.10-9.99 in 0.01 sec. steps
Zone-3 direction	Z3FR	FWD/REV
Pos. Seq. line impedance angle	PANG	40-90, in 1.0 degree steps
Zero Seq. line impedance angle	GANG	40-90, in 1.0 degree steps
ZOL/Z1L	ZR	0.1-7.0, in 0.1 steps
Low Voltage unit	LV	40-60 in 1.0V (rms) steps
Overcurrent units		
Low set phase	IL	0.5-10, in 0.1 A steps
Med. set phase	IM	0.5-10, in 0.1 A steps
Low set ground	IOS	0.5-10, in 0.1 A steps
Med. set ground	IOM	0.5-10, in 0.1 A steps
High set phase	ITP	OUT, 2-150.0, 0.5 A steps
High set ground	ITG	OUT, 2-150.0, 0.5 A steps
Out-of-step block	OSB	YES/NO
OSB override timer	OSOT	400-4000 in 16 ms steps
OSB inner blinder	RT	1.00-15.00, in 0.10 Ω steps
OSB outer blinder	RU	3.00-15.00, in 0.10 Ω steps
Directional overcurrent, zero or negative sequence	DIRU	ZSEQ/NSEQ/DUAL
Directional overcurrent ground backup time curve family	GBCV	OUT, CO2,5,6,7,8,9,11
Ground backup pick-up	GBPU	0.5-4.0, in 0.1 A steps
Ground backup time curves within family	GTC	1-63, in 1.0 steps
Choice of directional or non-directional ground backup	GDIR	YES/NO

* *Optional*

TABLE 4-1. SETTING DISPLAY (SHEET 3 OF 3)

Information/Settings	Displayed at Function Field	Value Field (using 5 A ct and 60 Hz) (SEE NOTE)
CIF trip/stub bus protection	CIF	CIFT/STUB/BOTH/NO
LLT trip	LLT	YES/FDOG/NO
LOP block	LOPB	YES/NO
LOI Block	LOIB	YES/NO
Alarm 2 (Trip) Seal-In	AL2S	YES/NO
Remote Setting	SETR	YES/NO
Real Time Clock	TIME	YES/NO
1. Set Year	YEAR	1980-2079, in 1 year steps
2. Set Month	MNTH	1-12, in 1 month steps
3. Set Day	DAY	1-31 in 1 day steps
4. Set Weekday	WDAY	Sun, Mon, Tues, Wed, Thur, Fri, Sat
5. Set Hour	HOUR	0-24, in 1 hour steps
6. Set Minute	MIN	0-60, in 1 minute steps

NOTE: WHEN THE CTYP FUNCTION IS SET AT 1 AMPERE, THE RANGE OF THE FOLLOWING FUNCTIONS ARE AS SHOWN BELOW:

- ZIP/ZIG/Z2P/Z2G Z3P/Z3G/PLTP/PLTG 0.05-250.00, in 0.05 Ω steps
- ITP/ITG 0.4-30.0, in 0.1 A steps
- IL/IM/IOS/IOM 0.1-2.0, in 0.02 A steps

NOTE: SEE ALSO SECTION 5.2.4, SELECTIONS OF CTYP SETTINGS.

NOTE: SEE PREFACE FOR INFORMATION ON SETTING NOMENCLATURE APPLIQUES.

NOTE: The increments of timers are based on the line frequency, e.g., 16 msec for 60 Hz and 20 msec for 50 Hz (to the nearest msec)

TABLE 4-2. METERING DISPLAY

Information	Displayed at Function Field	Value Field
Phase A current (mag.)	IA	numerical, A (X.X)
Phase A current (ang.)	∠IA	deg. (X.X)
Phase A voltage (mag.)	VAG	numerical, v (XX.X)
Phase A voltage (ang.)	∠VAG	deg. (XX)
Phase B current (mag.)	IB	(0.0)
Phase B current (ang.)	∠IB	(0)
Phase B voltage (mag.)	VBG	(0.0)
Phase B voltage (deg.)	∠VBG	(0)
Phase C current (mag.)	IC	(0.0)
Phase C current (ang.)	∠IC	(0)
Phase C voltage (mag.)	VCG	(0.0)
Phase C voltage (ang.)	∠VCG	(0)
Month / Day	DATE	numerical (00.00)
Hour / Minute	TIME	numerical (00.00)
Local/Remote Setting	SET	LOC/REM/BOTH
Carrier Receive -1	RX1	YES/NO
Carrier Receive -2	RX2	YES/NO
LOP indication	LOP	YES/NO
LOI indication	LOI	YES/NO
Out-of-Step Block	OSB	YES/NO
Rotation of Phase Sequence	ROT	JABC/JACB

TABLE 4-3. TARGET (FAULT DATA) DISPLAY (SHEET 1 OF 2)

Information	Displayed at Function Field	Displayed at Value Field
Month / Day	DATE	XX.XX
Year	YEAR	XXXX
Hour / Minute	TIME	XX.XX
Second	SEC	XX.XX
Fault type	FTYP	AG/BG/CG/AB/BC/CA/ ABG/BCG/CAG/ABC
BKR.#1 ϕA tripped	BK1A	YES/NO
BKR.#1 ϕB tripped	BK1B	YES/NO
BKR.#1 ϕC tripped	BK1C	YES/NO
BKR.#2 ϕA tripped	BK2A	YES/NO
BKR.#2 ϕB tripped	BK2B	YES/NO
BKR.#2 ϕC tripped	BK2C	YES/NO
Zone-1 phase tripped	Z1P	YES/NO
Zone-1 ground tripped	Z1G	YES/NO
Zone-2 phase tripped	Z2P	YES/NO
Zone-2 ground tripped	Z2G	YES/NO
Zone-3 phase tripped	Z3P	YES/NO
Zone-3 ground tripped	Z3G	YES/NO
Pilot phase tripped	PLTP	YES/NO
Pilot ground tripped	PLTG	YES/NO
High set phase tripped	ITP	YES/NO
High set ground tripped	ITG	YES/NO
Close-into fault trip	CIF	YES/NO
Load-loss tripped	LLT	YES/NO
Ground backup tripped	GB	YES/NO
SPF tripped (SPF)	SPT[1]	YES/NO
62T tripped (SPT)	62T[1]	YES/NO
Fault location	Z	(In ohms)
Fault Z angle	FANG	(numerical)
Fault distance	DMI or DKM	(in miles or KM)
Prefault load current	PFLC	numerical, A
Prefault phase voltage	PFLV	numerical V
Prefault load angle	LP	numerical deg.
Carrier send	SEND	YES/NO
Receiver #1	RX1	YES/NO
Receiver #2	RX2	YES/NO
Weakfeed tripped	WFT	YES/NO

1 Optional

TABLE 4-3. TARGET (FAULT DATA) DISPLAY (SHEET 2 OF 2)

Information	Displayed at Function Field		Value Field
Fault type	FTYP		AG/BG/CB/AB/BC/CA ABG/BCG/CAG/ABC
Fault voltage VA (mag.)	VPA		numerical, V
	(ang.)	∠VPA	numerical deg.
Fault voltage VB(mag.)		VPB	numerical V
	(ang.)	∠VPB	numerical deg.
Fault voltage VC(mag.)		VPC	numerical V
	(ang.)	∠VPC	numerical deg.
Fault voltage 3V0(mag.)		3VO	numerical V
	(ang.)	∠3VO	numerical deg.
Fault voltage IA(mag.)		IPA	numerical A
	(deg.)	∠IPA	numerical deg.
Fault voltage IB(mag.)		IPB	numerical A
	(deg.)	∠IPB	numerical deg.
Fault voltage IC(mag.)		IPC	numerical A
	(deg.)	∠IPC	numerical deg.
Fault Current 3I0 (mag)		3I0	numerical A
	(deg.)	∠3I0	numerical deg.
Pol. current IP(mag.)		IP	numerical A
	(deg.)	∠IP	numerical deg.
Month/Day		DATE	XX.XX
Year		YEAR	1980-2079
Hour/Minute		TIME	XX.XX
Second		SEC	XX.XX

TABLE 4-4. RECOMMENDED JUMPER POSITIONS (V2.1X)

OUTER CHASSIS

An External jumper between FT-Switch 13 and 14 of 2FT-14 should be connected permanently. (**Refer to terminals 2 & 4 of 2 FT-14 on Figure 4-3**.)

INTERCONNECT Module

JMP 1 to 6, & 13	For the rated input dc voltage
JMP 7 & 9	For Stub Bus Protection
JMP 8 & 10	For the trip alarm (AL2-2)
JMP 11 & 12	For MDAR with FT switches only

MICROPROCESSOR Module

JUMPER	POSITION	FUNCTION
JMP 1	1-2	EEPROM (8kx8)
JMP 2	2-3	Single-pole trip option
JMP 2	1-2	Three pole trip or Programmable contact outputs
JMP 3	OUT	Standard for Rotation ABC
JMP 3	IN	Rotation ACB
JMP 4	OUT	No dropout time delay for trip contacts
JMP 5	OUT	Disable output contact test
JMP 6	OUT	Normal operation
JMP 8 & 9	1-2	RAM (32kx8)
JMP 10, 11 & 12	IN/OUT	Spare jumpers

POWER SUPPLY Module

JMP1	1-2	Carrier Stop	NO
	2-3	Carrier Stop	NC
JMP2	1-2	Carrier Send	NO
	2-3	Carrier Send	NC

CONTACT Module (Optional)

JMP1	NO	OC-5 Contact, NO
	NC	OC-5 Contact, NC
JMP2	NO	OC-6 Contact, NO
	NC	OC-6 Contact, NC
JMP3	NO	OC-7 Contact, NO
	NC	OC-7 Contact, NC
JMP4	NO	OC-8 Contact, NO
	NC	OC-8 Contact, NC

TABLE 4-5. OUTPUT CONTACT SELECTION

File Substation Communicate Relay Commands Help (Alt H) Sec

Type q or Q to quit changes: C8 DO 5000

Contact Output #	OR	A ND	CIFT	Z2PG	Z2G	Z3P	Z3G	GB	PLTG	PLTP	BC/G	IOS	FDOG	CG	OCSB	ECHOT	LLOA	LOPA	IT G	Z1G	Z1P	AB C	SEND	ABG/	LTX	AG	C A/G	ITP	TBM	CG	21R	BI
1	X			X	X	X	X																									
2																																
3																																
4	X																			X	X											
5																																
6																																
7																																
8	X									X	X																					

Contact 4 Pickup Timer = 50 msec Contact 4 Dropout Timer = 100 msec
Contact 8 Pickup Timer = 100 msec Contact 8 Dropout Timer = 5000 msec

Use up, down, right, left arrows, Ins or Del keys for logic or Enter for timers.
Note: In Pott scheme, ECHO is weakfeed or'd with open bkr key
Note: In Block Scheme, substitute STOP for ECHO; LLT is LLT or'd with WFT

Alt + D - Devices Alt + P - Pri/Sec 10/22/92 COM1 = 1200

Sub: Beaver Valley Substation 001 MDAR

NOTE: Refer to Table 3-4 for Description of Function.

Section 5. SETTING CALCULATIONS

WARNING

Check jumper #3 on the Microprocessor module for phase sequence rotation ABC or ACB. Remove jumper #3 for system ABC rotation. Refer to Section 1.8 for ACB system.

5.26 CALCULATION OF MDAR SETTINGS

The following MDAR setting calculations correspond to the setting categories in the **Installation Section 4.** Assume that the protected line has the following data:

- 18.27 miles
- Line reactance 0.8 ohms/mile
- 69 kV, 60 cycles
- Positive and negative sequence impedances:

  $ZIL(Pri) = Z2L(Pri) = 15\angle 77^\circ$ ohms

- Zero sequence impedance: /
  $Z_{0L}(pri) = 50\angle 73^\circ$ ohms

- Current Transformer Ratio (CTR):
  RC = 1200/5 = 240 (Set CTR = 240)
- Voltage Transformer Ratio (VTR):
  RV = 600/1 = 600 (Set VTR = 600)

- Relay secondary ohmic impedances are:

  $Z = Z_{pri} \times R_C/R_V$

  $Z_{1L} = Z_{2L} = 15\angle 77^\circ \times 240/600 = 6\angle 77^\circ$ ohms

  $Z_{0L} = 50\angle 73^\circ \times 240/600 = 20\angle 73^\circ$ ohms

5.26.1 Ratio of Zero and Positive Sequence Impedances

$ZR = Z_{0L}/Z_{1L} = 20/6 = 3.33$

then MDAR will automatically calculate the zero sequence current compensation factor (k_0) by using the value of ZR, PANG, GANG and equation (1) in **section 3.2.1**, i.e.,

$k_o = (Z_{0L} - Z_{1L})/Z_{1L} = ZR \angle(GANG-PANG)-1$

5.26.2 Zone-1 Distance Unit Settings

A setting of 80% of the line impedance for zone-1 reach is recommended, thus the Zone-1 phase and ground reach should be:

Z1P = 6 x 0.8 = 4.8 and
Z1G = 6 x 0.8 = 4.8

NOTE: Z1P and Z1G can be set for different values if the application is required. Refer to Section H, Step 10 for calculation and example.

5.26.3 Zone-2 and Pilot Distance Unit Settings

Generally, Zone-2 reach is set for 100% of the protected line plus 50% of the shortest adjacent line, For this example, if the shortest (or only) adjacent line primary impedance is 20 ohms, then the Zone-2 reach setting would be:

Z2P = 6 + (20 x 0.5) x 240/600 = 10 and
Z2G = 10

The pilot zone distance phase and ground reaches can be set either exactly or nearly equal to the Zone-2 phase and ground distance reach, which depends on the application. For this example, set it equal to Zone-2 reach, i.e.,

PLTP = 10 and PLTG = 10

NOTE: Z2P, Z2G, PLTP and PLTG can be set for different values or disabled if the application is required.

5.26.4 Zone-3 Distance Unit Settings

Generally, Zone-3 reach is set to underreach of the shortest Zone-2 reach of the adjacent line off the remote bus. A practical setting is set for 100% of the protected line plus 100% of the shortest adjacent line off the remote bus. For example, if the shortest Zone-2 reach off the remote bus is 25 ohms primary, and infeed effect may increase its impedance by 30%, then the Zone-3 reach setting should be:

Z3P = 6 + (25 x 1.3) x 240/600 = 19 and
Z3G = 19

NOTE: Z3P and Z3G can be set for different values if the application is required.

5.26.5 Overcurrent Unit Setting

a. The low set phase overcurrent unit is used for supervising the load-loss-trip and CIF functions. It should be set higher than the line charging current and below the minimum load current.

NOTE: It should be set above the maximum tapped load current if applicable.

Assume that the line charging current is negligible for this line section, and the minimum load current is 2.0 A secondary, then the low set phase overcurrent unit setting should be:

IL = 1

b. The medium set phase overcurrent unit is used for supervising the OSB function and all the phase distance units. this unit should be set not to limit the Zone-3 reach, but traditionally, its setting should be set higher than load current.

Assume that 4.5 amperes has no effect to the Zone-3 reach, and the maximum load current is 4.0 amperes, then the medium set phase overcurrent unit can be set to:

IM = 4.5

c. The low-set ground overcurrent unit is used for supervising the reverse directional overcurrent ground unit (RDOG) for transient block in pilot system ad carrier SEND in Blocking system. It should be set as sensitive as possible. A setting of 0.5 amperes is recommended:

IOS = 0.5

d. The medium set ground overcurrent unit is used for supervising the trip of Zone-1, Zone-2 and Zone-3 ground distance units (Z1G, Z2G and Z3G), the forward directional overcurrent ground unit (FDOG). Generally, it is recommended to be set 2 times the IOS setting.

IOM = 2 x IOS = 1.0

e. The directional high set overcurrent phase and ground units (ITP and ITG) are used for direct trip function. The general setting criterion for the instantaneous direct trip unit is:

The unit should be set higher than 1.15 times the maximum fault on the remote bus, where the factor of 1.15 is to allow for the transient overreach. For this example, assume that the maximum load is not higher than the maximum forward end zone fault current, and the maximum phase and ground fault currents on the remote bus are 20 and 24 amperes, respectively, then the settings of the high-set phase (ITP) and the high-set ground (ITG) should be:

ITP = 20 x 1.15 = 23

ITG = 24 x 1.15 = 27.6

5.26.6 OSB Blinder Settings (RT and RU)

The requirements for setting the blinder units are:

- Inner blinder must be set to accommodate maximum fault resistance for internal 3-phase fault
- Inner blinder should not operate on severe stable swings
- Outer blinder must have adequate separation from inner blinder for fastest out-of-step swing to be acknowledged as an out-of-step condition
- Outer blinder must not operate on load

a. Setting the Inner Blinder (21BI)

If the OSB is used to supervise tripping of the 3ϕ unit on heavy load current, the inner blinder 21BI must be set sufficiently far apart to accommodate the maximum fault arc resistance. A reasonable approximation of arc resistance at fault inception is 400 volts per foot. If a maximum ratio of “line voltage per spacing” is 10,000 volts/ft. for a high voltage transmission line, and if a minimum internal 3-phase fault current is calculated as:

$$I_{min.} = [E / 1.73(Z_A+Z_L)]$$

where Z_A is maximum equivalent source impedance, Z_L is line impedance and E is line-to-line voltage.

then $R_{max.} = 400 \times FT / I_{min.}$

$$= 400x1.73(Z_A+Z_L)/10000$$

$$= 0.0693 (Z_A+Z_L)$$

Adding a 50% margin to cover the inaccuracies of this expression:

$$R_{max.} = 0.104(Z_A+Z_L) \text{ primary ohms}$$

$$R_S = 0.104(Z_A+Z_L)R_C/R_V \text{ secondary ohms}$$

Set inner blinder to:

$$R_T = R_S \times \cos(90° - PANG) \quad (1)$$

This is the minimum permissible inner blinder setting when it is used to provide a restricted trip area for a distance relay.

Another criterion that may be considered is based upon the rule of thumb that stable swings will not involve an angular separation between generator voltages in excess of 120°. This would give an approximate maximum of:

$$Z_{inner} = (Z_A+Z_L+Z_B)/(2\times1.73) \quad (2)$$

$$= 0.288(Z_A+Z_L+Z_B) \text{ primary ohms}$$

$$Z_{inner} = 0.288(Z_A+Z_L+Z_B)R_C/R_V \text{ secondary ohm}$$

where Z_B is the equivalent maximum source impedance at the end of the line away from Z_A.

An inner blinder setting between the extremes of equations (1) and (2) may be used. This provides operation for any 3-phase fault with arc resistance, and restraint for any stable swing. Except in those cases where very fast out-of-step swings are expected, the larger setting can be used.

It will usually be possible to use the minimum inner blinder setting of 1.5 ohms.

b. Setting the Outer Blinder (21BO)

For slow out-of-step swings, a reasonably close placement of outer to inner blinder characteristic is possible. The separation must, however, be based on the fastest out-of-step swing expected. A 50 ms interval is inherent in the out-of-step sensing logic, and the outer blinder must operate 50 ms or more ahead of the inner blinder.

Since the rate of change of the ohmic value manifested to the blinder elements is dependent upon accelerating power and system WR^2, it is impossible to generalize. However, based on an inertia constant (H) equal to 3, and the severe assumption of full load rejection, a machine will experience (assuming a uniform acceleration) an angular change in position of no more than 20° per cycle on the first half slip cycle.

If the inner blinder were set for ($0.104Z_T$), and the very severe 20° per cycle swing rate were used, the outer blinder should be set for approximately:

$$Z_{outer} = 0.5\ Z_T \text{ primary ohms} \quad (3)$$

where $Z_T = Z_A + Z_B + Z_L$

This is the minimum setting of the outer blinder for a 20° per cycle swing rate.

For example, if $Z_{inner} = 0.104\ Z_T$, $Z_{outer} = 0.5\ Z_T$, RT = 1.5

$$\frac{Z_{outer}}{Z_{inner}} = \frac{0.500}{0.104} = 4.8$$

$$\frac{Z_{outter}}{Z_{inner}} = \frac{R_U}{R_T} = 4.8$$

$$R_U = 4.8 \times 1.5 = 7.2$$

5.26.7 Overcurrent Ground Backup Unit (GB)

The overcurrent ground backup unit GB provides seven sets of curves, which are similar to the CO and MCO curves, for backing up the distance ground on high resistance ground faults. Four settings (GBCV, GBPU, GTC and GDIR) should be determined for applying this unit.

a. GBCV is the ground backup curve selection. Seven sets of familiar CO curves are provided (CO2,5,6,7,8,9 and 11), and are shown in **Figures 2-1 thru 2-7**. The selection is based on the application and coordination time. A selection of “OUT” disables the ground backup function.

b. GBPU is the current level setting. Its range is 0.5 to 4.0 amperes in 0.5 steps. In general, the current level setting criterion is:

$(I_{Fmin}/2)$ > Setting level > 2 x (Max. residual load, $3I_0$)

where I_{Fmin} = Minimum ground fault current for a fault two buses away

For better sensitivity, GBPU should be set at 0.5 amperes, this would be adequate for most of the application.

c. GTC is the time delay setting of the GB unit. As shown in **Figures 2-1 thru 2-7**, it has 63 setting selections, from 1 to 63 in 1.0 steps. In general, the

time delay setting should be coordinated with any protective device downstream of the line section.

The following equation can be used to calculate the trip time for all CO curves from CO-2 thru CO-11 :

$$T\ (sec) = \left[T_0 + \frac{K}{(3I_0 - C)^P}\right] \times \frac{GTC}{24,000} \quad (for\ 3I_0 \geq 1.5)$$

$$T\ (sec) = \frac{R}{(3I_0 - 1)} \times \frac{GTC}{24,000} \quad (for\ 1<3I_0< 1.5)$$

Where $3I_0 = \frac{I_F}{GBPU}$

GBPU = Pickup current setting (0.5 to 4.0A).

GTC = Time curve dial setting (1 to 63).

T_0, K, C, P and R are constants, and are shown in **Table 5-3**. (Refer also to the example in **Appendix H, Section 1.1.9**.)

d. GDIR is the setting for directional control selection. The GB unit will become a directional torque control overcurrent ground unit if GDIR is set at YES.

e. DIRU controls the setting of the directional polarizing ground overcurrent unit. It has 3 selections:

ZSEQ — Zero sequence voltage polarization only.

DUAL — Both zero sequence voltage and current polarizations.

NSEQ — Negative sequence voltage and current operated.

Taking the CO-8 curve set as an example (**see Figure 2-5**), assuming that the maximum 3Io of unbalanced load is 0.2A, the minimum ground fault current for a fault two buses away is 10A, and 0.7 seconds is required for coordination with current of 20 times the GBPU setting, then the settings of the GB function should be as shown below:

10/2 > GB > 2 x 0.2 set GBPU = 0.5

Using the curve in **Figure 2-1**, for 0.7 seconds at 20 times the GBPU setting, GTC should be set to 24.

- Set GBCV = C0-8 and
- Set GDIR = YES if directional control is required.
- Set DIRU = ZSEQ

5.26.8 Timer Settings

a. Zone-2 timer (T2) setting should be coordinated with the Zone-1 and other high-speed trip units on the adjacent line terminal. Coordination Time Interval (CTI) of 0.3 to 0.5 seconds is recommended. For example, if T2 of 0.4 seconds is used, then the phase and ground Zone-2 timers should be set as follows:

T2P = 0.4 and T2G = 0.4

NOTE: T2P and T2G are separate timers; they can be set at different time settings.

b. Zone-3 timer (T3) settings would be similar to the above. For example, if T3 of 0.8 seconds is required, then the phase and ground Zone-3 timer should be set as follows:

T3P = 0.8 and T3G = 0.8

NOTE: T3P and T3G are separate timers; they can be set at a different time settings.

c. For out-of-step block (OSB), if applied, the OSB override timer setting (OSOT) is determined by the power system operation. Its range is 400 to 4000 ms, in 16 ms steps. For example, set MDAR OSOT = 500 if OSB override time of 500 ms is required.

d. For single-pole trip application only, the single phasing limit timer setting (62T) is for preventing thermal damage to rotating machines, due to the I_2 component during single phasing. Its range is 300 to 5000 ms. in 50 ms steps. The setting should be based on the poorest $(I_2)^2t$ constant of the machines in service. For example, set MDAR 62T = 1550, if 3PT is required before 1.55 seconds and after one pole has been open and the breaker does not or cannot reclose.

e. For the blocking system only, the channel coordination timer setting (BLKT) is based on the following application criteria:

BLKT > (Slowest remote carrier start time + channel time + margin) - (the fastest local 21P/21NP pickup time)

Where channel time includes the transmitter and receiver times, and the times which occur between these devices, e.g., wave propagation, interfacing relays, etc.

For MDAR:

fastest 21P/21NP pickup time	=	14 ms
slowest carrier start time	=	4 ms
suggested margin time	=	2 ms

For example, the MDAR channel coordination timer should be determined as shown below, if the channel time is 3 ms.

$$BLKT = (4 + 3 + 2) - 14 = -5$$

i.e., set BLKT = 0

5.27 SELECTION OF MDAR SETTINGS

The following settings are determined by the application. They do not require calculation.

5.27.1 The OSC setting is for selecting one of the 4 ways (TRIP/Z2TR/Z2Z3/ΔIΔV) to initiate the oscillographic data taken, where:

TRIP — start data taken only if trip action occurs.

Z2TR — start data taken if Zone-2 units pick up, or any trip action occurs.

Z2Z3 — start data taken if Zone-2 or Zone-3 units pick up, or any trip action occurs.

ΔIΔV — start data taken if ΔI, ΔV, Zone-2 or Zone-3 units pick up, or any trip action occurs.

NOTE: The setting of ΔI, ΔV, for OSC is not recommended.

5.27.2 The FDAT setting is for selecting one of the 3 ways (TRIP/Z2TR/Z2Z3) to initiate the fault data taken, where:

TRIP — start to store fault data only if trip action occurs.

Z2TR — start to store fault data if Zone-2 units pick up or any trip action occurs.

Z2Z3— start to store fault data if Zone-2 or Zone-3 units pick up or any trip action occurs.

5.27.3 The current transformer ratio setting (CTR**)** is used for the load current monitoring, if it is selected to be displayed in primary amperes. It has no effect on the protective relaying system. For this example, set CTR = 240.

5.27.4 The voltage transformer ratio setting (VTR) is used for the system voltage monitoring, if it is selected to be displayed in primary volts. It has no effect on the protective relaying system. For this example, set VTR = 600.

5.27.5 The frequency setting (FREQ) should be selected to match the power system operating frequency. For example, select FREQ = 60 if the power system operating frequency is 60 Hertz.

5.27.6 The current transformer type setting (CTYP) provides the flexibility for 5 Amp or 1 Amp rated current transformer selection. For example, select and set CTYP = 5 if a 5 Amp current transformer is used.

The setting of CTYP affects all the distance unit and overcurrent unit setting ranges. The ranges will be automatically changed as listed in **Table 5-1**.

5.27.7 The read primary setting (RP) should be set at YES if all the monitoring ac voltages and currents are selected to be displayed in primary KV and KA values, respectively.

5.27.8 The ohms per unit distance of the line reactance setting (XPUD) is the multiplier for fault distance display. It has a range of 0.3 to 1.5 in 0.001 steps. In this example, the line reactance is 0.8 ohms/mile; set XPUD = 0.8.

The fault distance calculation is as follows:

$$DMI = \frac{VTR}{CTR} \times \frac{Z_S \times \sin\angle FANG}{XPUD}$$

Where Z_S is the secondary impedance magnitude, and FANG is the fault angle.

5.27.9 The setting of DTYP (distance type DKM & DMI) has a selection of MILE and KM. It should be selected to match with the setting of XPUD. For this example, select DTYP = MILE.

5.27.10 The setting of TTYP is for selecting the reclosing mode in single pole trip applications (if applicable). It has six selecting positions (OFF, 1PR, 2PR, 3PR, SPR, and SR3R). Refer to the guidelines for reclosing mode programming for the TTYP setting selection.

5.27.11 For an SPT application, set the 62T single phasing limit timer from 300 to 5000 ms in 50 ms steps. The setting is based on the

generator's $(I_2)^2t$ performance. LV should be set between 85% and 90% of the rated line-to-neutral voltage.

5.27.12 The settings of Z1RI, Z2RI and Z3RI provide the selectivity for Zone-1 RI (reclosing initiation), Zone-2 RI and Zone-3 RI, respectively. For the non-pilot system application, set Z1RI, Z2RI and/or Z3RI to YES, if RI is required when the particular distance zone operates. For the pilot reclosing, Z1RI should be set to "YES".

5.27.13 For a pilot system, set BFRB to YES if RB on the breaker failure squelch feature is required.

5.27.14 The setting of PLT (pilot) combines with the signal of Pilot Enable (on the backplane panel) and controls the operation of pilot and reclosing initiation. The absence of either signal will:

- disable the pilot system
- block the RI2 output, and
- allow an RI1 output for a non-pilot system.

The PLT can be set either locally from the front panel or, remotely, via the communication channel.

5.27.15 The STYP (system type) selects the desired relaying system for the application. It has two selections: 3ZNP (3-zone non-pilot) and Z1E (Zone-1 extension) in the non-pilot MDAR. There are five selections: 3ZNP, Z1E, POTT (permissive overreach transfer trip or unblocking), PUTT (permissive underreach transfer trip) and BLK (blocking) in the pilot MDAR. It should be set to the desired selection.

5.27.16 For the pilot MDAR only, the WFEN (weakfeed enable) selection should be set to YES for the weakfeed terminal, if applicable.

5.27.17 For permissive pilot MDAR only, the 3TRM (3 terminals) setting should be selected to YES for all of the POTT/PUTT three terminals that apply, but for the BLK system the "YES" or "NO" makes no difference. **Refer to section 3.21 for the detailed information**.

5.27.18 For application of POTT/BLK systems, the transient block logic is always in the POTT/BLK system, but it is initiated by the reverse looking units. The Z3FR setting should be set to "YES" and Z3P, Z3G should be set to 100% of the line impedance.

5.27.19 The FDGT (FDOG trip delay timer) can be set from 0 to 15 cycles or block (BLK) as desired. It is recommended to set to 3 cycles or longer. **Refer to Section 3.9** for the detailed FDGT information.

5.27.20 Distance/overcurrent units can be disabled if required by the application. The following distance/overcurrent units can be disabled by setting the unit to OUT:

a. List of units which can be disabled:

PLTP, PLTG, Z1P, Z2P, Z2G, Z3P, Z3G, ITP, ITG and GB.

b. Procedure to disable the unit:

Switch MDAR to the setting mode, scrolling the function field to the proper function Then set the unit to OUT via the value field.

5.27.21 Set T1 to YES if Zone-1 delay trip is required.

5.27.22 The T2P, T2G, T3P and/or T3G timer functions can be disabled, if desired, by setting the timer to BLK.

5.27.23 The Zone-3 distance units (Z3P and Z3G) can be selected to reach forward-looking or reverse-looking by setting the Z3FR (Zone-3 forward or reverse) to FWD or REV. For pilot application, Z3FR must be set to REV.

5.27.24 Set the positive sequence impedance angle (PANG) value based on the positive sequence line impedance angle. This setting affects the performance of the distance units.

5.27.25 Set the zero sequence impedance angle (GANG) value based on the zero sequence line impedance angle. This setting affects the performance of the distance units.

5.27.26 Set the ZR value based on the absolute value of the ratio of the line impedances (Z_{OL}/Z_{1L}).

5.27.27 The LV units are used in CIFT, SPT and weakfeed logic in the MDAR. They should normally be set to 40 volts unless a higher

setting is required for more sensitive applications. **Refer to Section 5.2.11** for the SPT application.

5.27.28 The polarizing approach for the directional ground overcurrent unit is controlled by the setting of DIRU. It has 3 selections:

ZSEQ — Voltage polarization only.

DUAL — Both voltage and current polarization.

NSEQ — Negative sequence voltage and current polarization.

5.27.29 Set GDIR to YES if directional control is required for the GB function.

5.27.30 Based on the requirements, set Close-Into-Fault (CIF) and stub-bus protection functions, by selecting the value field (CIFT/STUB/BOTH/NO) of CIF, where:

CIFT — CIF trip but not stub-bus protection has been selected.

STUB — Stub-bus protection but not CIF trip has been selected.

BOTH — Both CIF trip and stub-bus protection have been selected.

NO — Neither CIF nor stub-bus protection has been selected.

Set LLT (loss-of-load trip) to YES, FDOG or NO, where:

YES — LLT trip with Z2 supervision.

FDOG — LLT trip with both Z2 and FDOG supervision.

NO — LLT trip function is not used.

5.27.31 Set LOPB to YES, if loss-of-potential block trip function is required.

5.27.32 Set LOIB to YES, if loss-of-current block trip function is required.

5.27.33 Set AL2S to YES, if trip alarm seal-in is required. The Reset pushbutton can be used to reset the sealed AL2.

5.27.34 Set the SETR to YES if remote setting is required.

5.27.35 Procedure to set the real-time clock:

5.27.36 With MDAR in the "setting" mode, scroll the function field to TIME, and set the value to YES. Depress function pushbutton RAISE to display YEAR, MNTH (month, DAY, WDAY (week day), HOUR, and MIN (minute), and set the corresponding number via the value field. The MDAR clock will start at the time when the minute value is entered.

5.28 GUIDANCE FOR RECLOSING INITIATION MODE PROGRAMMING

5.28.1 For system without SPT system:

a. Select TTYP = OFF or 1PR, or 2PR or 3PR, and

b. Select PLT = NO, and

c. Use the RI2 output contact for the reclosing circuit, and

d. Select one or all of the Z1RI, Z2RI and Z3RI to YES, depending on the application.

5.28.2 For system with SPT system:

a. Select TTYP = OFF or 1PR, or 2PR, or 3PR, or SPR or SR3R and

b. Select one or all of the Z1RI, Z2RI and Z3RI to YES, depending on the application.

c. Use the RI1 output contact for the SRI reclosing timing circuit, and the RI2 output contact for the 3RI timing circuit.

The Reclosing Initiation mode will be based on the TTYP setting, as shown in **Table 5-2**.

5.29 SELECTION OF PROGRAMMABLE CONTACTS

Thirty signals have been pre-assigned as shown in Table 3-4 and **Figure 3-33**. The 4 heavy duty contacts (OC1 to OC4) connected to FT switches and 4 standard contacts (OC5 to OC8) can be selected from the 30 signals by ANDing or ORing them together. The selection can only be done from WRELCOM® Communication Channel. Contacts OC4 and OC8 provide timers for delay pickup and/or delay dropout. The ranges of timers are 0 to 5 seconds in 0.01 second steps.

TABLE 5-1. CURRENT TRANSFORMER SETTINGS

MDAR UNITS	At CTYP = 5	At CTYP = 1
Z1P/Z1G/Z2P/Z2G Z3P/Z3G/PLTP/PLTG	0.01-50.00, in 0.01 Ω steps	0.05-250, in 0.05 Ω steps
ITP/ITG	2.0-150.00, in 0.5 A steps	0.4-30.0. in 0.1 A steps
IL/IOS/IOM	0.5-10.0, in 0.1A steps	0.1-2.0, in 0.02 A steps

TABLE 5-2. RECLOSING INITIATION MODE PROGRAMMING

TTYP	TYPE OF FAULT	RECLOSING MODE
OFF	all	no reclosing
1PR	ϕG Other Faults	RI2 contact closes; no reclosing
2PR	ϕG, ϕϕ 3ϕ	RI2 contact closes; no reclosing
3PR	all	RI2 contact closes
SPR	Phase-to-ground Other Faults	RI1 contact closes; no reclosing
SR3R	Phase-to-ground Other Faults	RI1 contact closes; RI2 contact closes

TABLE 5-3. TRIP TIME CONSTANTS FOR CURVES

CURVE #	T_0	K	C	P	R
C02	111.99	735.00	0.675	1	501
C05	8196.67	13768.94	1.13	1	22705
C06	784.52	671.01	1.19	1	1475
C07	524.84	3120.56	0.8	1	2491
C08	477.84	4122.08	1.27	1	9200
C09	310.01	2756.06	1.35	1	9342
C011	110	17640.00	0.5	2	8875

Appendix A. BACKPLANE MODULE

All external electrical connections pass thru the Backplate (**see Figure 4-1)** of the outer chassis. If the MDAR is used without the FT-14 switch, six 14-terminal connectors on the Backplane module (TB1 thru TB6) are used. If the FT-14 switch (option) is included (using the two peripheral areas of the MDAR cabinet), then only four of the 14-terminal connectors (TB2 thru TB5) are used. Three DIN connectors, (J11, J12, J13) allow for the removal of the outer chassis (Backplane module) from the inner chassis (Interconnect module).

Electrical inputs to the Backplane module, which are routed either directly thru the Backplate or through the FT-14 switch to the Backplate, include:

- V_A, V_B, V_C, and V_N (70 V_{AN})
- I_A/I_{AR}, I_B/I_{BR}, I_C/I_{CR}, and I_P/I_n
- BP(48, 125 or 250 Vdc) and BN (common)

The Backplane module, (**see Figure A-1** and Schematic) contains three voltage-type transformers, (TX1, TX2, TX3) for V_A/V_N (V_{AN}), V_B/V_N (V_{BN}), V_C/V_N (V_{CN}) inputs.

A Transformer module (**see Figure A-2** and Schematic) is piggybacked onto the Backplane module, consisting of four current-type transformers (I_A, I_B, I_C and I_N) with four 0.1% resistors. The primary windings of all seven transformers are directly-connected to the input terminal (TB6/1 thru 12); the secondary windings are connected thru the Interconnect module to the Filter module. The current transformers (I_A, I_B, I_C and I_N) are not gapped; dc offset attenuation is done with a digital filtering algorithm. They drive resistive burdens to develop a proportional voltage. Surge suppression is included where the signals enter and exit the case.

The Backplane module also includes:

- 2 chokes (L1 and L2) for dc power supply filter
- 48 surge-suppressor type capacitors

The D-connector, with 9 terminals on the Backplane module, is used for the INCOM®/PONI (Product Operated Network Interface) communications box. INCOM®/PONI is supplied in two versions:

- RS232C to INCOM
- INCOM/PONI to INCOM® network interface (supplied as option).

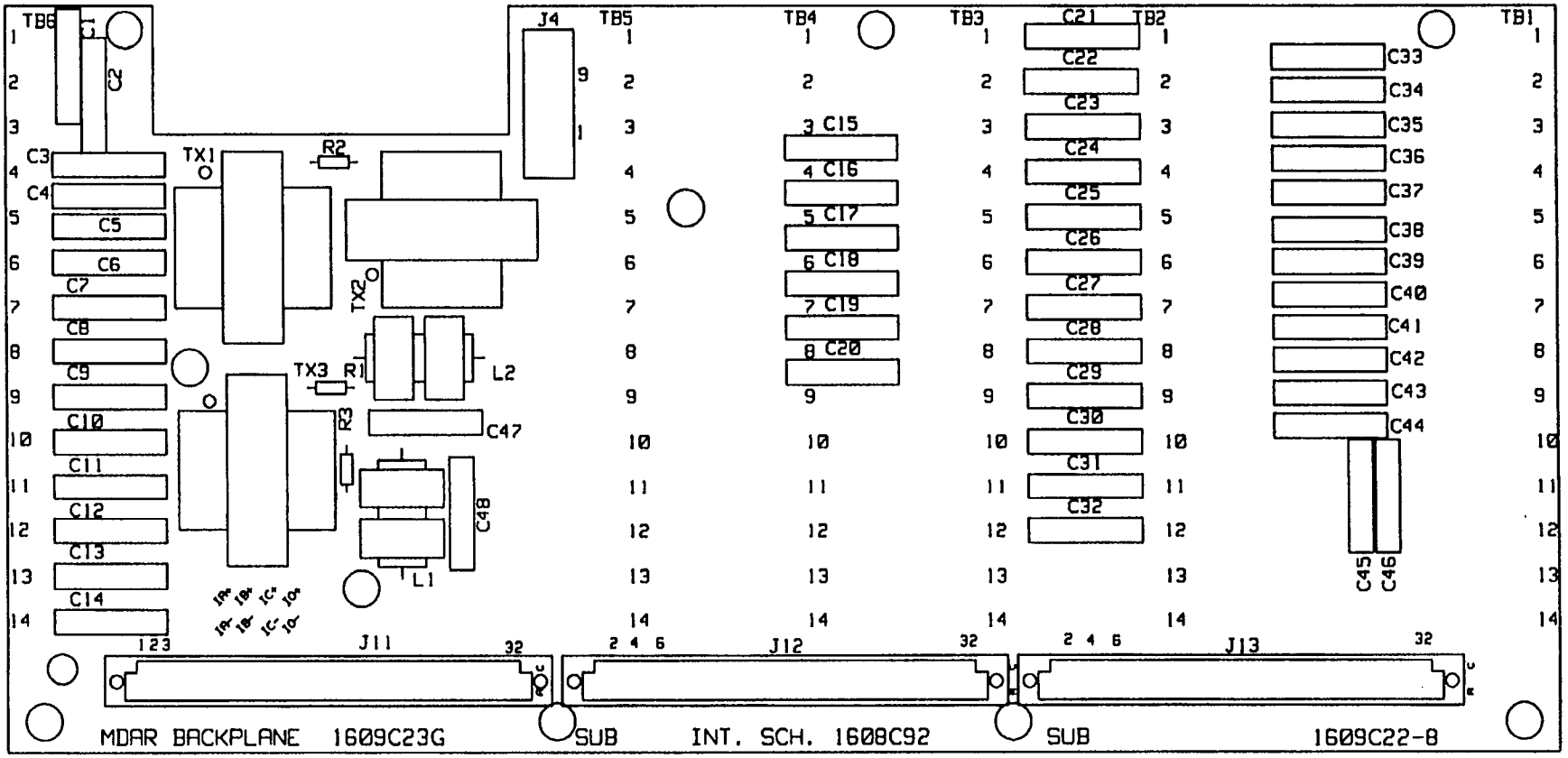


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Figure A-1 MDAR Backplane Module PC Board (sheet 3 of 3)

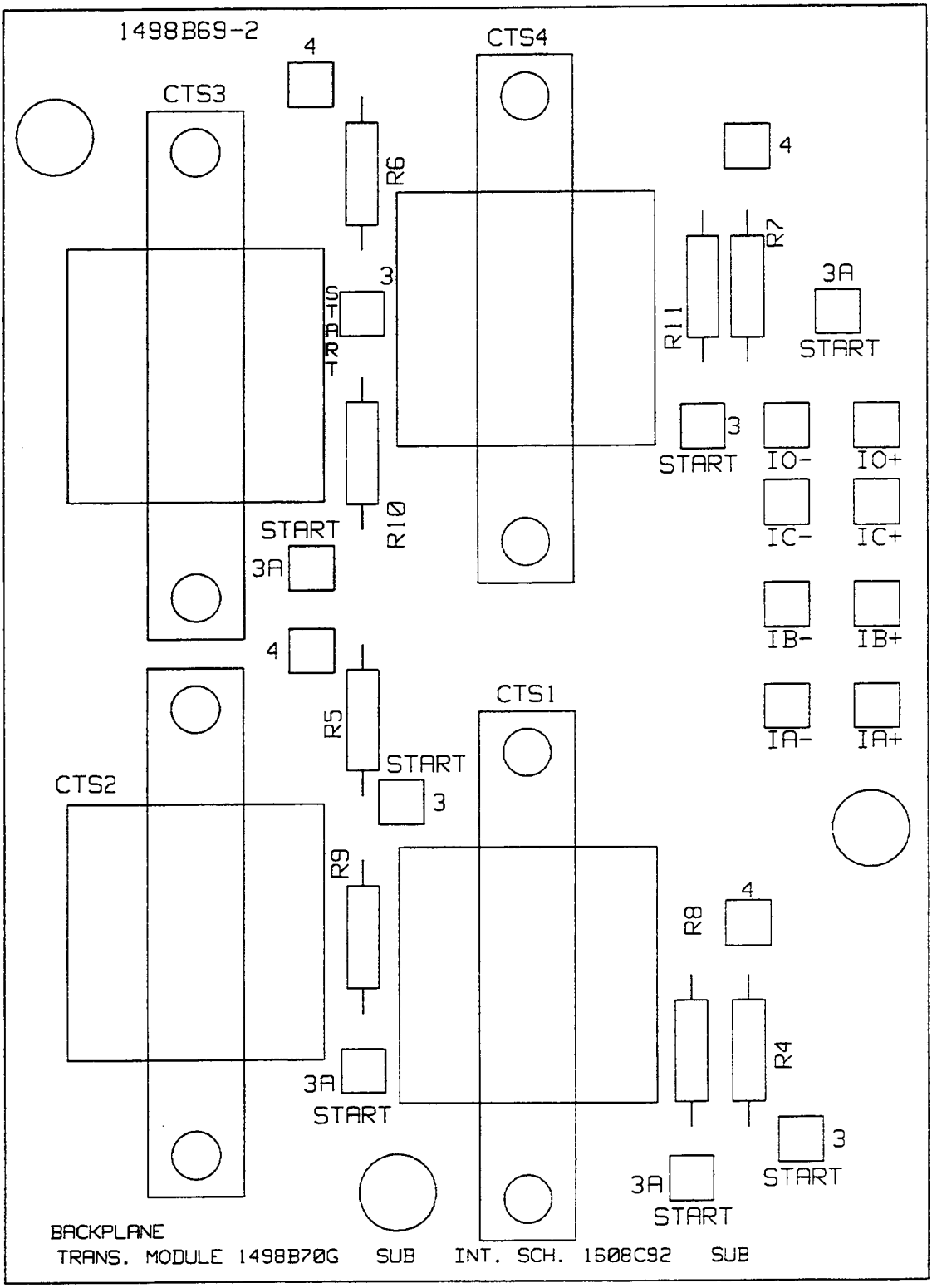
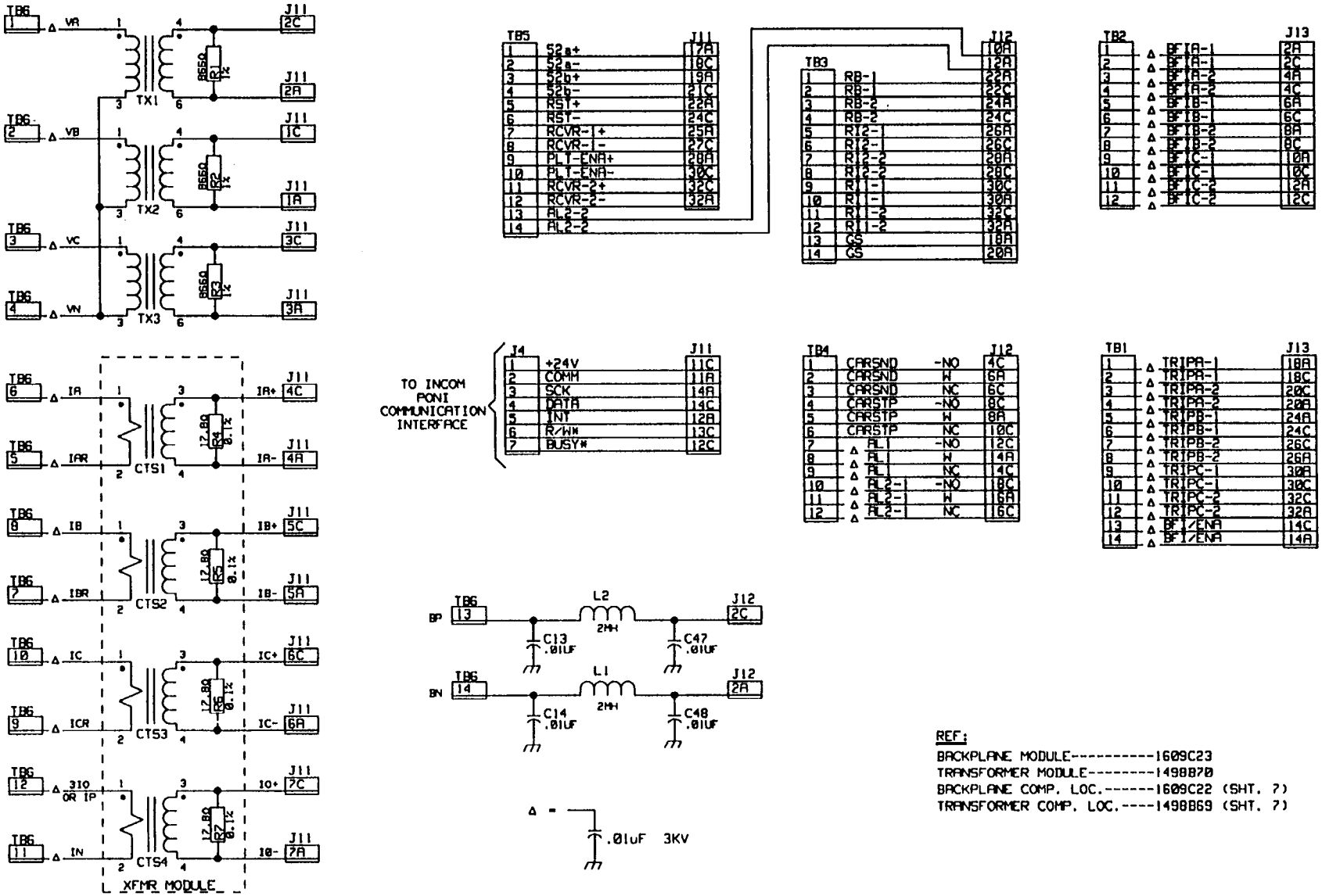


Figure A-2 MDAR Backplane/Transformer Module PC Board.



Sub 5
1608C92

Figure A-3 MDAR Backplane/Transformer Module Schematic.

MDAR BACKPLANE MODULE 1609C23 **SUB 13**

	5 AMP CT		G01
	1 AMP CT		G02
	PC BOARD SUB 11	1609C22	ALL

LOCATION	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1 thru C48	.01 UF 20% 3000V Z5U CERAMIC DISC	3536A32H02	01,02,03
CHOKES			
L1	2.0MH 1.3MHZ 0.8A	3500A27H01	01,02,03
L2	2.0MH 1.3MHZ 0.8A	3500A27H01	01,02,03
CONNECTORS			
J4	RS232C 9 Pin	9650A08H01	01,02,03
J11	64 Pin	1496B47H02	01,02,03
INDUCTOR			
L1, 2	2MH IHA-1-01	3500A27H01	01,02,03
SOCKET CON			
J12, 13	64 Pin	9646A11H03	01,02,03
TRANSFS			
TX1, 2, 3	PC-4-2173B	1496B50H04	01,02,03

Appendix B. INTERCONNECT MODULE

The Interconnect module (**see Figure B-1** and Schematic) becomes the floor of the MDAR chassis and provides electrical connectors for all other modules; it connects (thru J11, J12 and J13) from the Backplane module (at the rear), to the Filter and Power Supply modules (at the left and right sides, respectively), to the Option (single-pole trip) module (at the center if used), and to the Microprocessor and Display modules at the front of the chassis. The components on the Interconnect module include:

- 2 dc power fuses
- 7 optical isolators
- 2 alarm relays

The seven optical isolators are identical in design. Each input jumper (JMP1 thru JMP6 and JMP 13) can be placed in one of three positions, depending on the input voltage:

- Position 1 (220 or 250 Vdc)
- Position 2[1] (48 or 125 Vdc)
- Position 3 (15 or 20 Vdc)

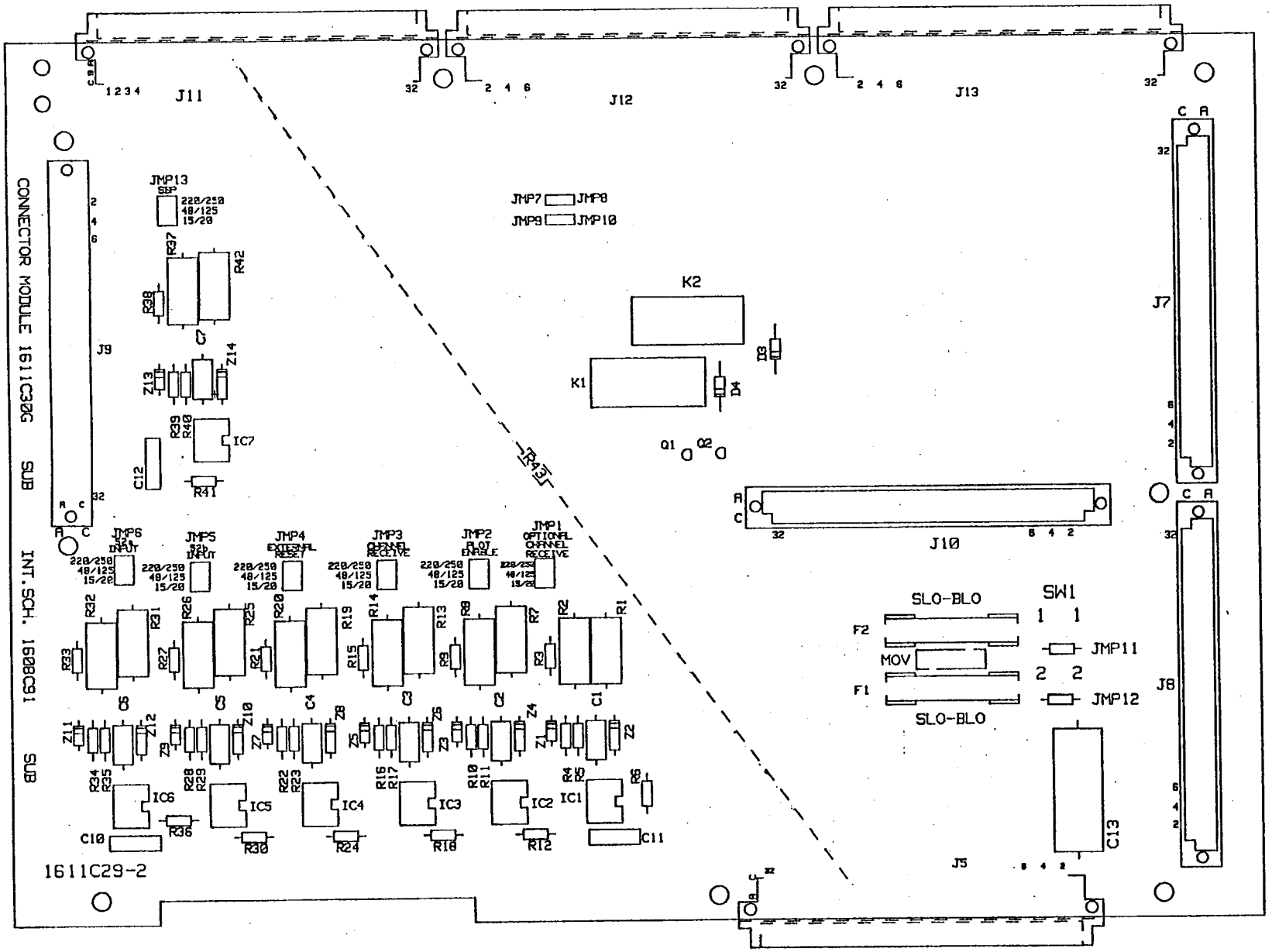
Voltage inputs are fed from the Backplane module to the Interconnect module; voltage outputs are fed from the Interconnect module to the Microprocessor module. Resistors, zener diodes, and capacitors are used as input buffers to protect the opto-coupler circuits (IC1 thru IC7) which provide 3500 Vdc isolation.

Two telephone-type relays are used as alarm 1 (K1) and alarm 2 (K2). The inputs are fed by the Microprocessor module; the outputs are connected to the output terminals of the Backplane module.

The second set of alarm 2 (AL2-2) is used only when the jumpers 8 and 10 are connected. Since the same Interconnect pc board terminals (10A and 12A) and Backplane terminals (TB5/13 and TB5/14) are use for either AL2-2 or Stub Bus Protection (SBP). For SBP application, move jumpers 8 and 10 to positions 7 and 9.

A resistor R43 is added in series between terminals J/524C and J11/14A for INCOM's SCK signal. The resistor R43 is in the INCOM clock line to stabilize the clock pulse.

[1] *Position 2 is the factory setting.*



Sub 6
1611C30

Figure B-1 MDAR Interconnect Module Component Location Diagram.

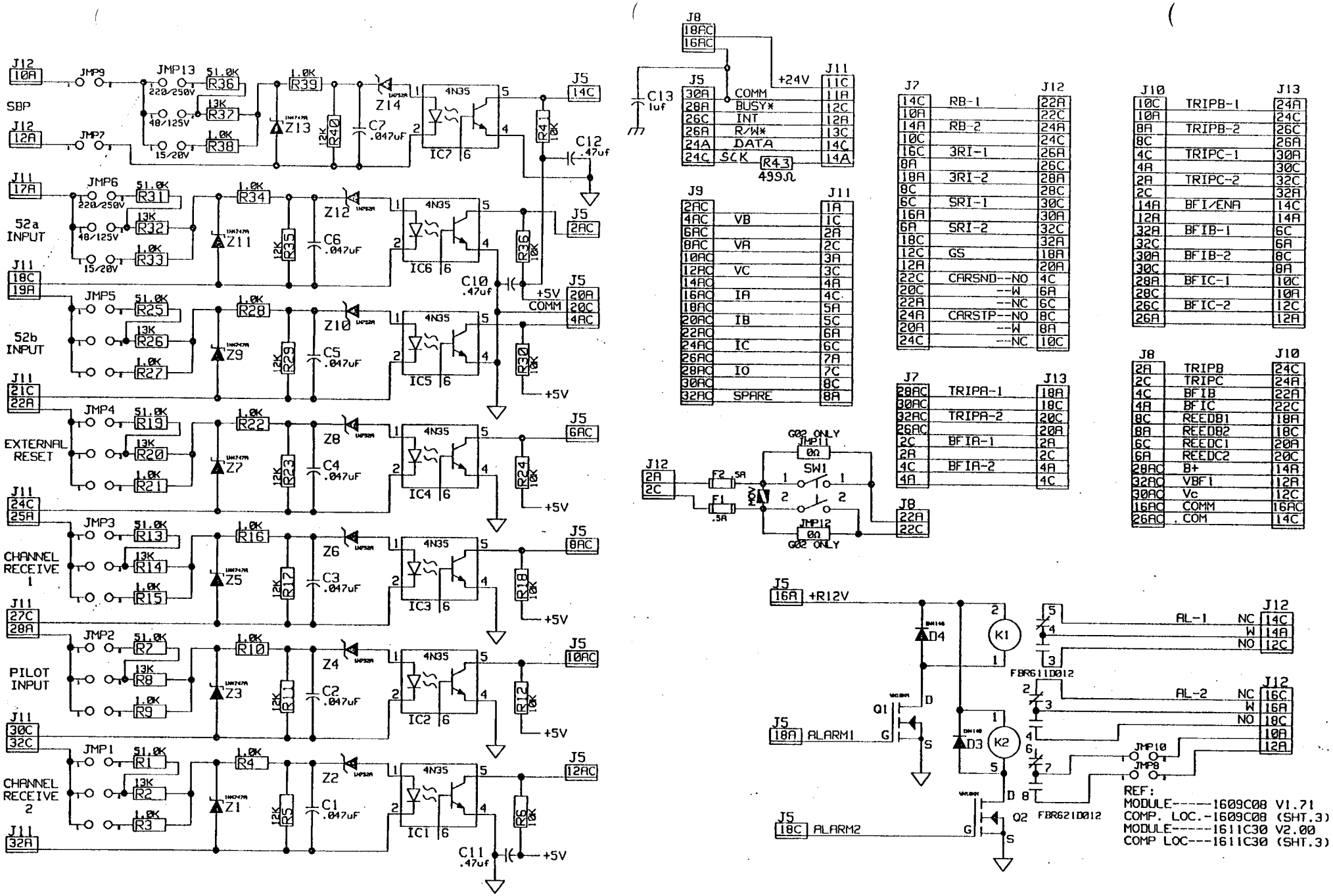


Figure B-2 MDAR Interconnect Module Schematic.

Sub 4
1608C91

MDAR INTERCONNECT MODULE 1611C30 SUB 9

	W/O FT-14 SWITCH W/ FT-14 SWITCH		G01 G02
PC BOARD	SUB 3	1611C29	ALL

COMP LOC	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1, 2, 3, 4, 5, 6, 7	.047uF 100V 5%	CF4702JL78	01, 02
C10, 11, 12	0.47uF 50V 20%	CP4703MH89	01, 02
C13	1MFD 400V 5%	CE1004JU53	01, 02
CONNECTORS			
JMP1, 2, 3, 4, 5, 6	3 POSITION	3532A49H01	01, 02
JMP7, 8, 9, 10	2 POSITION	9640A47H01	01, 02
J5, 12, 13	32 PIN	9646A11H02	01, 02
J7, 8, 9, 10	32 PIN	9646A11H03	01, 02
J11	64 PIN	1496B47HO1	01, 02
DIODES			
D3, 4	1N4148	836A928H06	01, 02
FUSES			
F1, 2	.5 AMP SLO-BLO	183A981H11	01, 02
JUMPERS			
JMP11, 12	0 OHMS	862A478H01	--- 02
OPTOELECTS			
IC1, 2, 3, 4, 5, 6, 7	4N35	774B936H01	01, 02
RELAYS			
K1	FBR611D012	9645A10H03	01, 02
K2	FBR621D012	9645A10H04	01, 02
RESISTORS			
R1, 7, 13, 19, 25, 31, 42	51.0K, 2W, 5%	RC5102J249	01, 02
R2, 8, 14, 20, 26, 32, 37	13.0K, 2W, 5%	RW1302J3F9	01, 02
R3, 4, 9, 10, 15, 16, 21, 22, 27, 28, 33, 34, 38, 39	1K .25W 1%	RM1001FQB0	01, 02
R5, 11, 17, 23, 29, 35, 40	12K .25W 1%	RM1212FQA9	01, 02
R6, 12, 18, 24, 30, 36, 41	10K .25W 1%	RM1002FQA9	01, 02
R43	499OHN .25W 1%	RM4990FQB1	01, 02
SOCKETS			
IC1, 2, 3, 4, 5, 6	6 PIN	3534A76H01	01, 02
TRANSISTORS			
Q1, 2	VN10KM N-MOSFET	9641A07H06	01, 02
VARISTORS			
MOV	ETZ-C140K391	3509A31H01	01, 02
ZENERS			
Z1, 3, 5, 7, 9, 11, 13	1N4747A	849A487H01	01, 02
Z2, 4, 6, 8, 10, 12, 14	1N752A	1861797H12	01, 02

Appendix C

OPTION MODULE
(For Single-pole Trip Application)

Schematic 1608C90-2
PC Board 1498B13-2
Parts List 1608C39-6

The Option module is mounted on the Interconnect module, at terminal connector J10, and is supported at the top by a central support bar.

This module (**see Figure C-1 and Schematic**) is designed for the single pole trip application. It provides two normally-open contacts for both B-phase tripping and C-phase tripping. It also provides breaker failure initiate signals. (Phase B and C circuits are identical; the Phase B circuit is described as an example.)

Terminal J10 (24C) provides a “TRIP B” signal from the Microprocessor module, through the Power Supply and Interconnect modules. Opto-Isolator (IC1) isolates the relay logic common from the battery common output. The trip condition occurs when signal “TRIPB”, at 5 Vdc, turns “ON” IC1 and Q1, which energizes trip relays (K1 and K2). Two reed relays (K3 and K4) are used to monitor the trip current. If a trip current is detected by “TRIP B-1”, relay (K3) is energized. The contact closure of “REED B-1” sends a signal to the Microprocessor (U100), through the Interconnect and Power Supply modules, and fault data is stored.

Similarly, the “BFIB” signal, at terminal J10 (22A) turns “ON” IC3 and Q3, and energizes telephone relay K9 if “VBFI” voltage (rated Vdc) exists. This voltage is controlled by a permanently-wired external jumper connected between terminals 13 and 14 of switch 2FT-14. (**See Block Diagram, 1609C25, at the end of the document.**) By opening switch 13 of 2FT-14, the VBFI signal is disconnected from B+ (but remains connected to switch 14 of 2FT-14); K9 will not pick up regardless of whether Q3 is “ON” or “OFF”.

The output contacts of the Option module are connected to terminal block (TB2) on the Backplate, through the Interconnect and Backplane modules.

CONTACT MODULE
(For Programmable Output Contact Application)

Schematic 1612C39-4
PC Board 9656A77-4
Parts List 1612C40-7

The Contact Module is mounted on the Interconnect Module at terminal J10 and is supported at the top by a central support bar.

This module is designed for the programmable output contacts (**See Figure C-1 and Schematic**). It provides four heavy duty contacts (OC1 to OC4) for tripping and four normal duty contacts (OC5 to OC8) for signal outputs. The OC5 to OC8 contacts can be set as normally open (NO) or normally closed (NC) contacts, depending on the positions of JMP1 to JMP4, respectively.

All eight circuits are independent and similar. Their input signals are from the Microprocessor Module through the Power Supply and Interconnect Modules. Opto-isolators U1 to U8 isolate the relay logic common (COMM) from the battery common (COM). Q1 to Q8 are used to drive the output relays K1 to K8, respectively. The eight contacts are connected to terminal block (TB2) on the backplate through the Interconnect and Backplate Modules.

Sub 2
1498B13

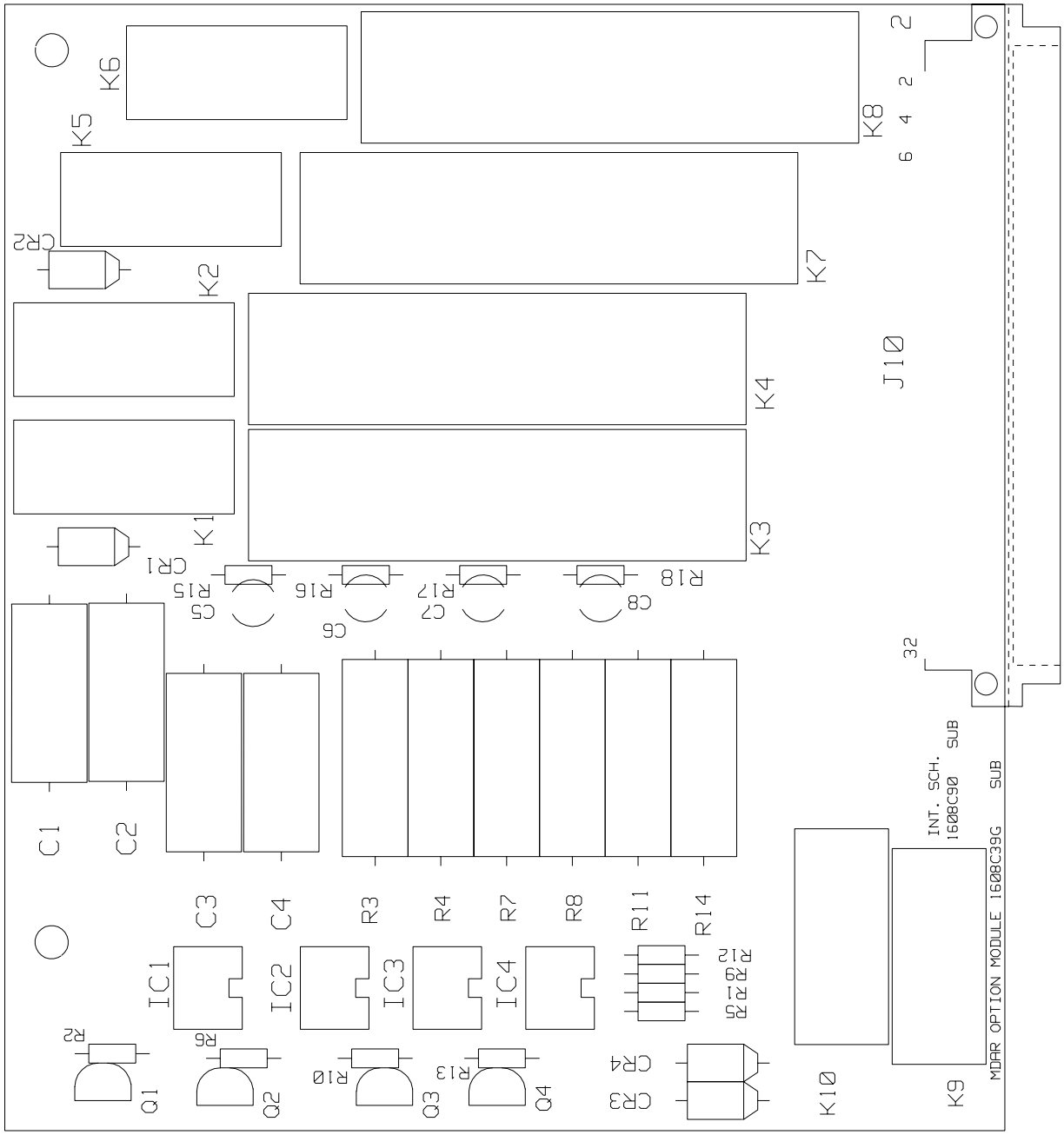


Figure C-1 MDAR Option Module

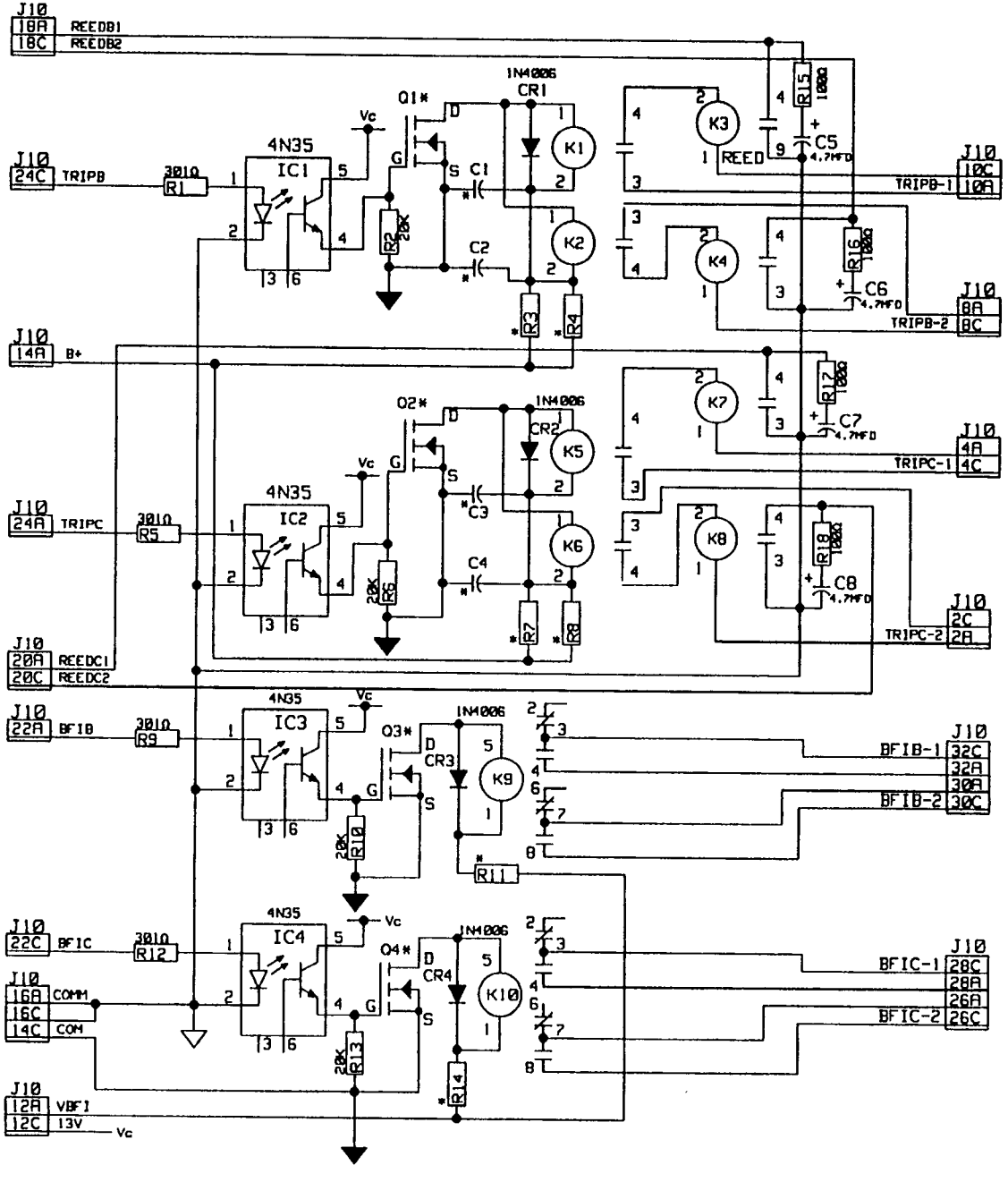


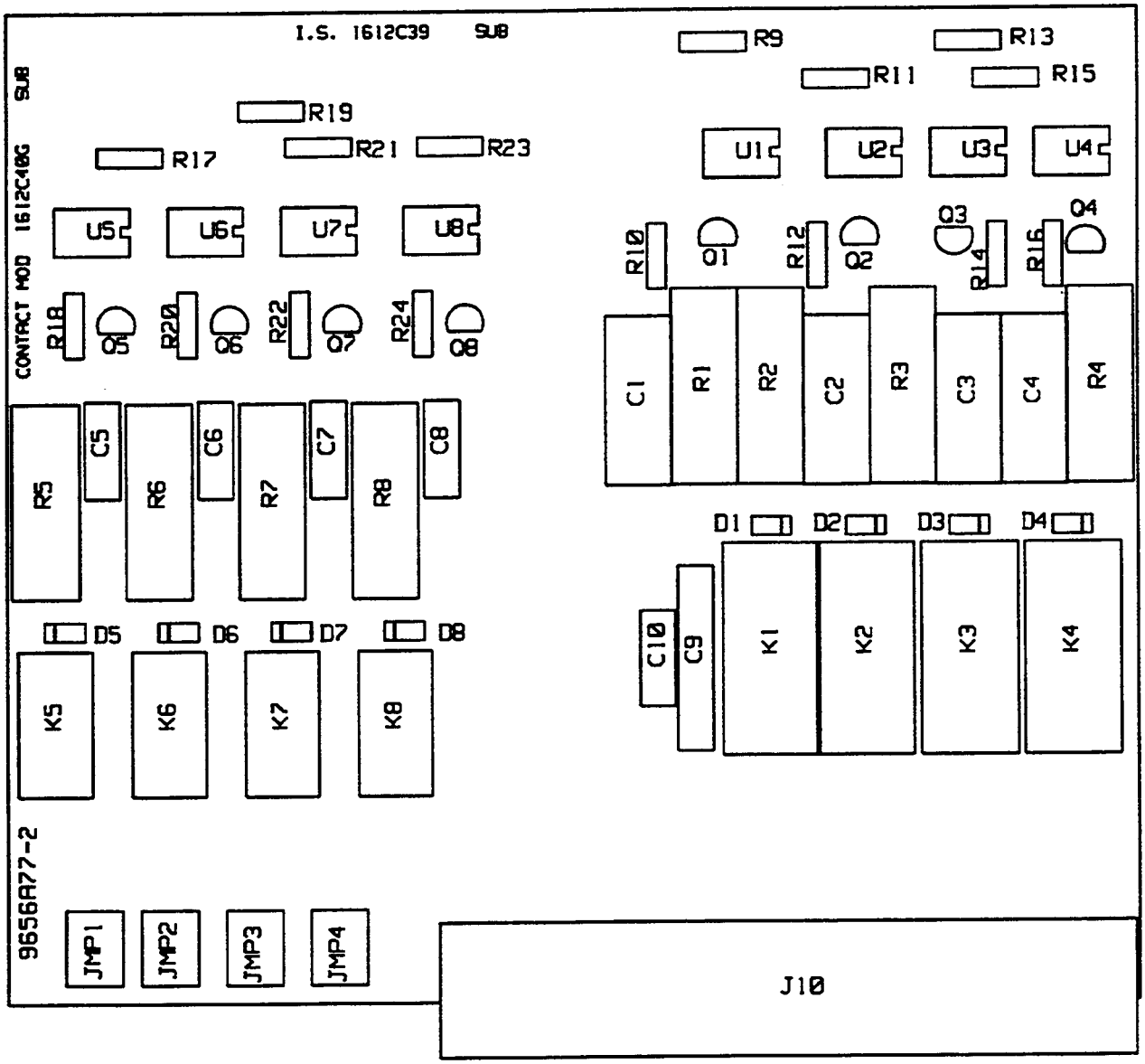
Figure C-2 MDAR Option Module Schematic

*= SEE CHART BELOW

COMPONENT	48V	125V	250V
R3 4 7 8 11 14	1K 5W	5K 5W	20K 5W
K1 2 5 6	RELAY 12V	RELAY 24V	RELAY 48V
K9 10	RELAY 24V	RELAY 24V	RELAY 24V
C1 2 3 4	1.0uf	1.0uf	0.47uf
Q1 2 3 4	VN2410M	VN2410M	ZVN0535A

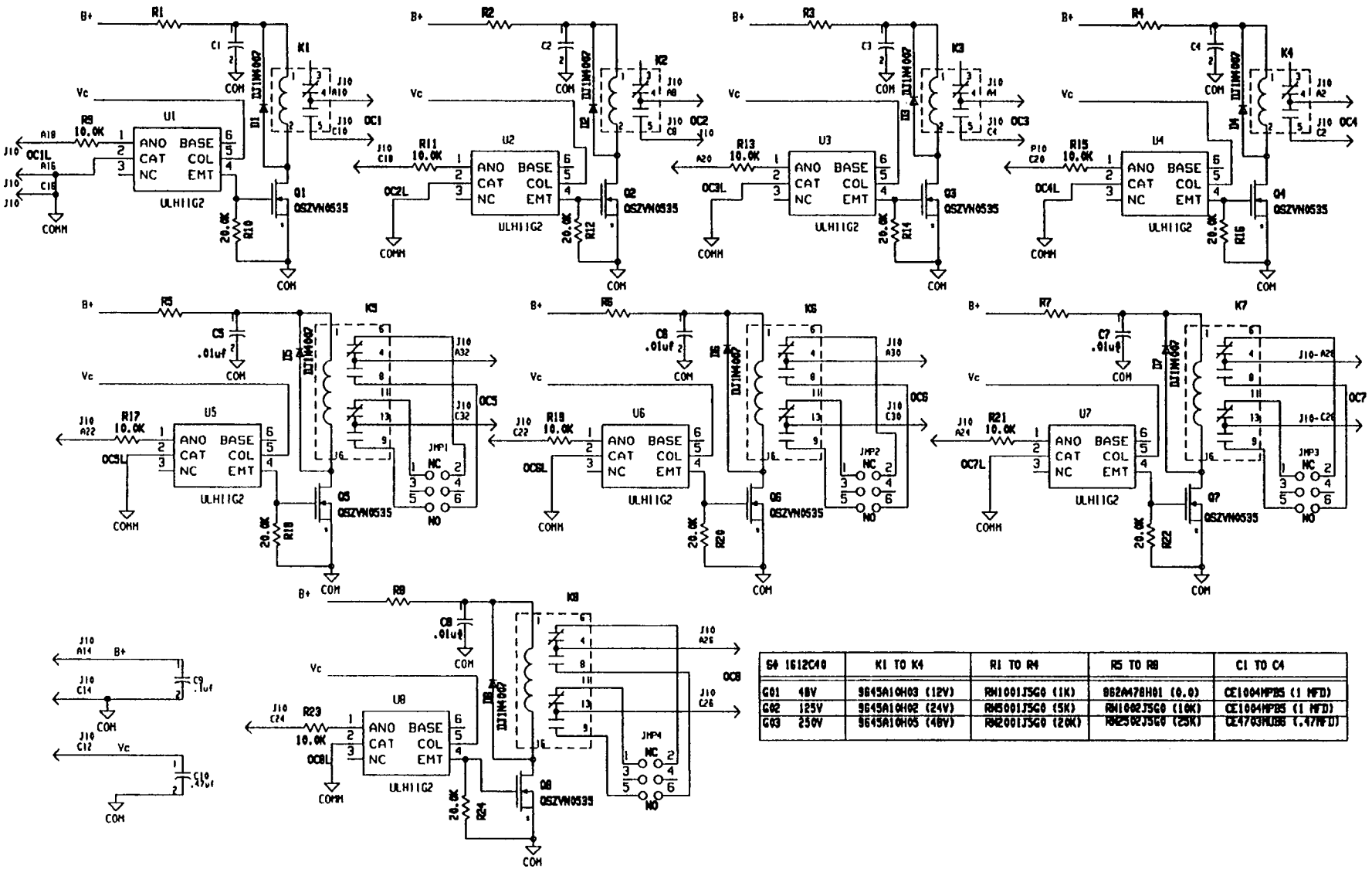
MODULE ASSEMBLY.....1608C39
COMPONENT LOCATION..1498B13 SHT.7

Sub 2
1608C90



Sub 2
9656A77

Figure C-3 MDAR Contact Module PC Board



G# 1612C40	K1 TO K4	R1 TO R4	R5 TO R8	C1 TO C4
G01 48V	9645A10H03 (12V)	RH1001J5G0 (1K)	0824478H01 (0.0)	CE1004MPB5 (1 MFD)
G02 125V	9645A10H02 (24V)	RH5001J5G0 (5K)	RH1002J5G0 (10K)	CE1004MPB5 (1 MFD)
G03 250V	9645A10H05 (48V)	RH2001J5G0 (20K)	RH2502J5G0 (25K)	CE4703MUB6 (.47MFD)

Sub 2
1612C39

Figure C-4 MDAR Contact Module Schematic

MDAR OPTION MODULE 1608C39 SUB 6

	48Vdc		G01
	125 Vdc		G02
	250 Vdc		G03
PC BOARD	SUB 2	1498B13	ALL

COMP LOC	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1, 2, 3, 4	1.0 MFD 200V	876A409H10	01,02
C1, 2, 3, 4	0.47 UF 400V	878A531H03	03
C5, 6, 7, 8	4.7 UF 50V	3533A75H02	01, 02, 03
CONNECTORS			
J10	RIGHT ANGLE 32P	9646A11H02	01,02,03
DIODES			
CR1, 2, 3, 4	1N5053	188A342H12	01,02,03
OPTOELECTS			
IC1, 2, 3, 4	4N35 OPTO-ISO.	774B936H01	01,02,03
REED RELAYS			
K3, 4, 7, 8	.5 AMP PICKUP	1442C62G01	01,02,03
RELAYS			
K1. 2, 5, 6	SPDT 12V 10A	9645A10H03	01
K9, 10	FBR621D024	9645A10H01	01, 02
K9, 10	FBR623D048	9645A10H06	03
RESISTORS			
R1, 5. 9, 12	301Ω .25W, 1% MF	3535A39H47	01,02,03
R2, 6, 10, 13	20K, .25W, 1% MF	3535A37H30	01,02,03
R3, 4, 7, 8, 11, 14	20K, 5W, 5%	763A129H08	03
R3, 4, 7, 8, 11, 14	1K, 5W, 5%	763A129H07	01
R15, 16, 17, 18	100Ω .25W, 1% MF	3535A39H01	01,02,03
TRANSISTORS			
Q1, 2, 3, 4	VN2410M	9455A42H51	01,02
Q1, 2, 3, 4	ZVN0535A N-MOSFET 350V 0.09A 50 OHM	9646A90H01	03

MDAR CONTACT MODULE 1612C40 **SUB 7**

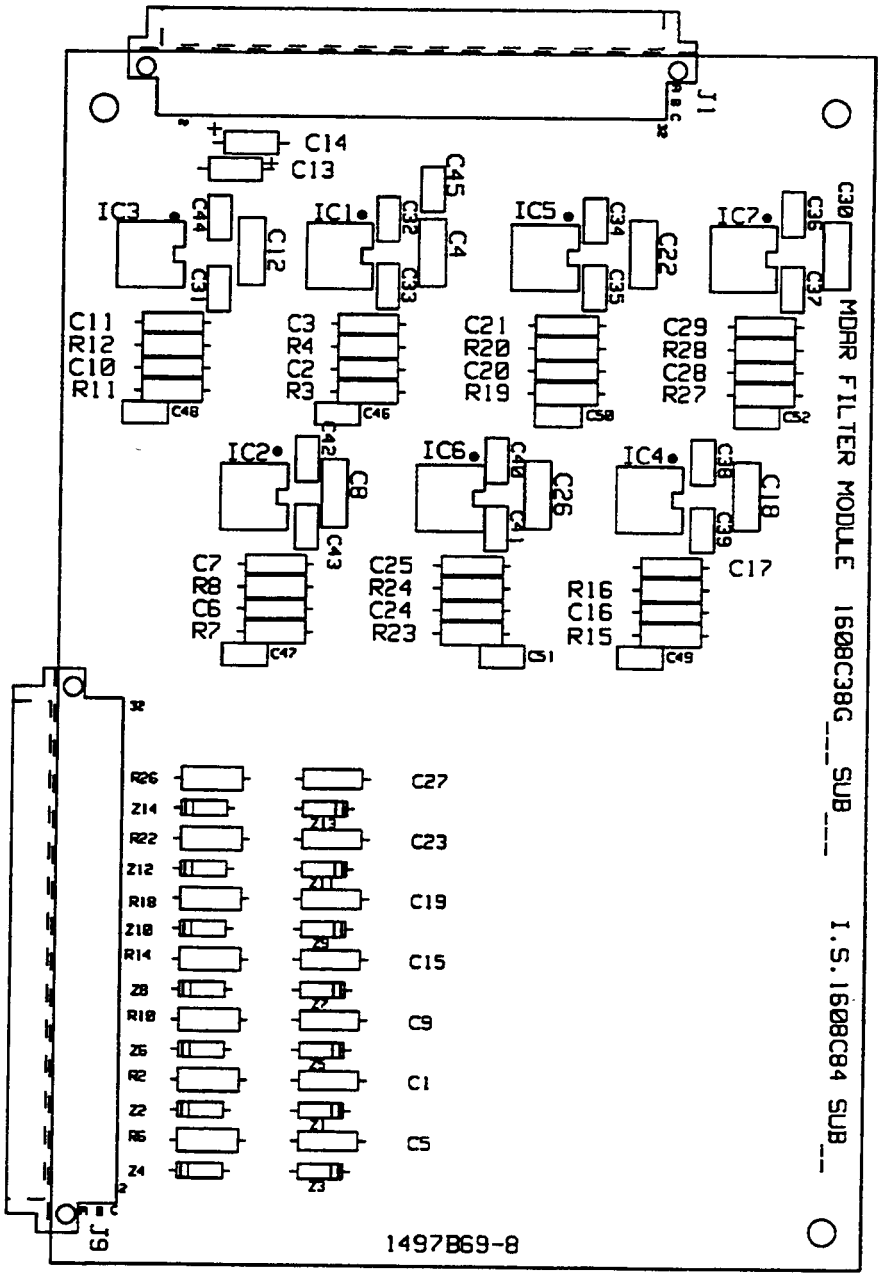
	48Vdc		G01
	125 Vdc		G02
	250 Vdc		G03
PC BOARD	SUB 4	9656A77	ALL

COMP LOC	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1, 2, 3, 4	0.47 UF 400V	CE4703MUB6	03
C1, 2, 3, 4	1.0 UF 5% 200V MET POLYESTER	CE1004MPB5	01,2
C5, 6, 7, 8	0.01 UF 20% 500V CERAMIC DISC	CQ1002MVB8	01,2,3
C9	0.1 UF 20% 500V CERAMIC DISC	CQ1003MV08	01,2,3
C10	0.47 UF 20% 50V Z5U MONO CERAMIC	CP4703MH89	01,2,3
CONNECTORS			
10	32 PIN DIN	9646A11H02	01,2,3
DIODE			
D1, 2, 3, 4, 5,6, 7, 8	1N4007 1000V 1A	836A928H08	01,2,3
OPTOELECT			
U1, 2, 3, 4, 5, 6, 7, 8	H11G2 OPTO ISOLATOR	1490B14H01	01,2,3
RESISTOR			
R1, 2, 3, 4	1K 5W	RW1001J5G0	01
R1, 2, 3, 4	20 KILOHMS 5W	RE2002J5G0	03
R5, 6, 7, 8	1.5 KILOHMS, 5%, I1W	RC1501J167	01
R5, 6, 7, 8	15 KILOHMS 5%, 10W	RW1502JAH2	03
R1, 2, 3, 4	5 KILOHMS 5% 5W WIREWOUND	RW5001J5G0	02
R5, 6, 7, 8	6 KILOHMS 5% 5W WIREWOUND	RW6001J5G0	02
R9, 11, 13, 15, 17, 19, 21, 23	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	01,2,3
R10, 12, 14, 16, 18, 20, 22, 24	20.0 KILOHMS 1% O.25 METAL FILM	RM2002J5G0	01,2,3
RELAY			
K5, 6, 7, 8	1600 OHMS 10% 24V 2 FORM C	3534A32H04	01,2,3
K1, 2, 3, 4	48V 1 FORM C	9645A10H05	03
K1, 2, 3, 4	24V 1 FORM C	9645A10H01	02
TRANSISTOR			
Q1, 2, 3, 4, 5, 6, 7, 8	ZVN053A N-MOSFET 350 0.09A 50 O	9646A90H01	01,2,3
HEADER			
6 PIN 3 POS		3532A49H01	01,2,3
JUMPER			
JMP1, 2, 3, 4	BLUE CHIP JUMPER	3532A54H01	01,2,3

Appendix D. FILTER MODULE

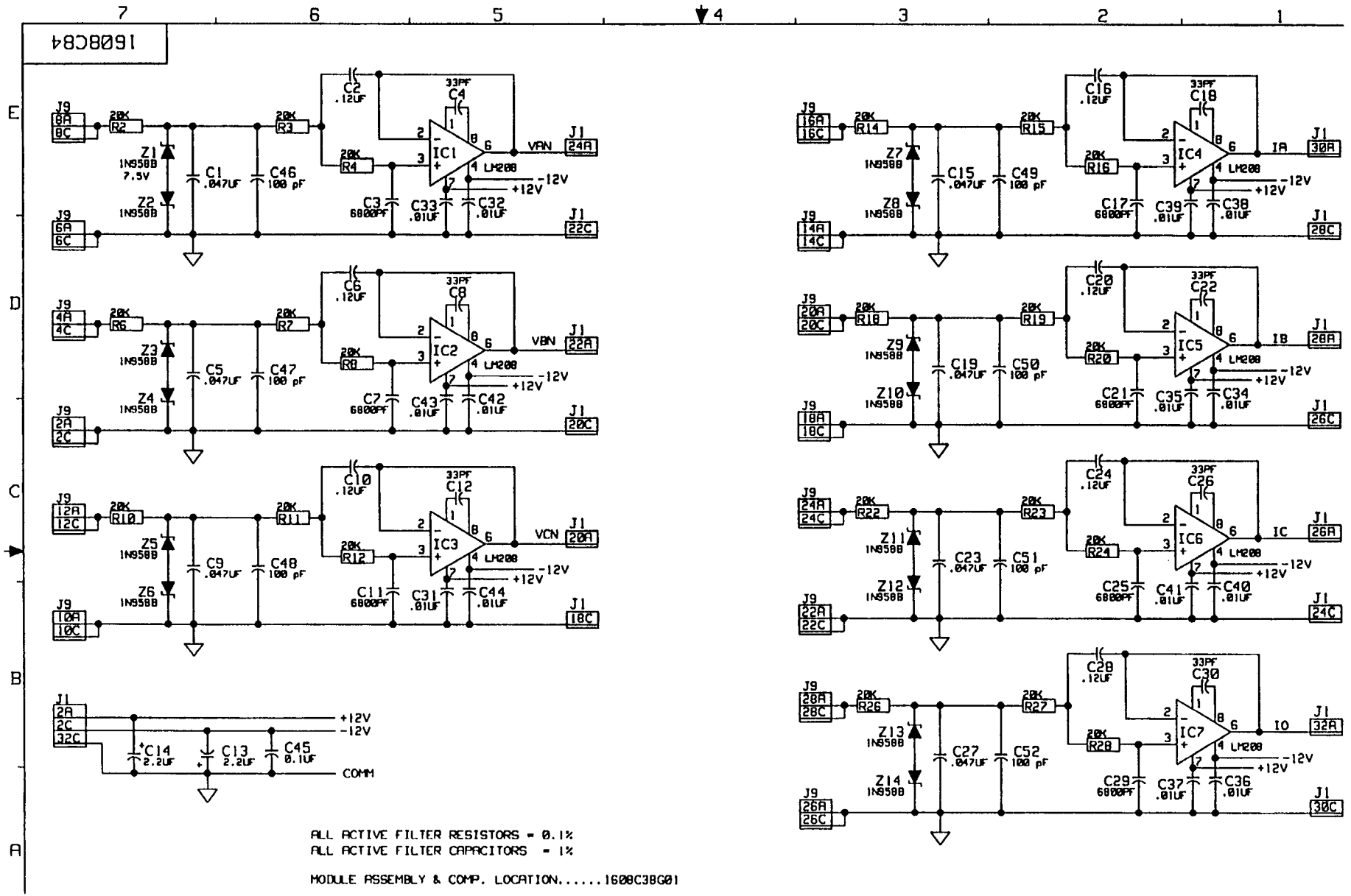
The Filter module (**see Figure D-1** and Schematic) consists of seven active lowpass Butterworth filters, which tend to band-limit the ac input signal prior to sampling and digitization. The filters are third-order Butterworth, with a cutoff frequency of 235 Hz (at -3 db). They coordinate with the Nyquist limit frequency of 240 Hz, determined by the 480 Hz sampling rate (8 samples per cycle) of the MDAR A/D converter.

Integrated circuits (IC1, IC2, IC3) are used for the inputs (V_{AN}, V_{BN}, V_{CN}); ICs (IC4, IC5, IC6, IC7) are used for input currents (I_A, I_B, I_C and I_N, respectively). All seven input signals are from the Interconnect module; the filter outputs are connected to the inputs of the analog signal multiplexer on the Microprocessor module.



Sub 7
1608C38

Figure D-1 MDAR Filter Module PC Board.



Sub 4
1608C84

Figure D-2 MDAR Filter Module Schematic.

MDAR FILTER ASSEMBLY 1608C38 SUB 9 4/93

PC BOARD SUB 8 1497B69 G01

COMP LOC	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1, 5, 9, 15, 19, 23, 27	.047UF 100V	CE4702FL61	01
C2, 6, 10, 16, 20, 24, 28	.12MFD 50V	CE1203FG61	01
C3, 7, 11, 17, 21, 25, 29	6800PF - 100V	CE1203FG61	01
C4, 8, 12, 18, 22, 26, 30	33PF - 500V	CR330AJV67	01
C13, 14	2.2UF 35V 5%	CJ2204JGA2	01
C31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44	.01UF	CP1002MHZZ	01
C45	0.1UF	CP1003ML89	01
C46, 47, 48, 49, 50, 51, 52	100 pF	CP1000KHZZ	01
CONNECTORS			
J1, 9	No description	9646A11H02	01
LINEAR ICS			
IC1, 2, 3, 4, 5, 6, 7	LM208J-8	9649A09H01	01
RESISTORS			
R2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27, 28	20K .1% .25W	RM2002C1A7	01
ZENERS			
CR1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	1N958B 7.5v	837A398H18	01

Appendix E. MICROPROCESSOR MODULE

The Microprocessor module controls the MDAR system (**see Figures E-1 and E-2**). A 16-bit addressable Microcontroller (INTEL 80C196) is used as the Microprocessor (U100), operating at 10 MHz frequency (**See Schematic, Sheet 1**). There are two programmable memories in separate, easily-replaceable EPROMs (U103, U104) and one Programmable Array Logic unit (PAL,U105). There are two read-write memories (RAMs, U200 and U201) for working storage, and one non-volatile RAM (NOVRAM, U202) for storing settings and targets (fault data) when the relay is deenergized.

Alarms 1 and 2 are located on the Interconnect module. The relays are both normally-open. Alarm-1 is used to signal a variety of failures; Alarm-2 signals the detection of a (TRIP) breaker circuit. Alarm-1 normally is energized (relay contact opens) when dc power is turned “ON”. It “drops out” (contact closes) when the Microprocessor module detects a failure in any of the following circuits:

- Microprocessor
- EPROM
- PROM
- RAM
- NOVRAM
- A/D Converter
- Digital I/O Circuitry
- DC Voltage Self-Check

Alarm-2 “picks up” (relay closes) when the breaker trip current is detected. Alarm-2 relay can be sealed-in if the setting of AL2S is “YES”.

A real-time clock (**U501, see Schematic, Sheet 2**), with back-up battery, can be set and synchronized externally through the INCOM/PONI card communication channel (**see Backplane module**), thru Microprocessor (U100).The time at fault is recorded on the fault data in memory. A program which interfaces the PONI card is included as part of the Microprocessor module.

An auto-ranging analog-to-digital conversion system includes an 8-channel multiplexer (MUX, U401). Three voltage inputs (V_A, V_B, V_C) and four current inputs (I_A, I_B, I_C, I_P)...(**See Schematic, Sheet 2**), are fed from the Filter module to the multiplexer. The eighth channel (I7) of the MUX (G23) allows for dc voltage self-check; it is monitored (by U300) for +5V or -6.8V. The control signals (MUX1, MUX2, and MUX4) select the channel input to be measured (via binary selection).

A sample-and-hold chip (U404) holds every input sample (sampled 8 times per power cycle) from the MUX for 80 microseconds. An analog switch (U300), used as an auto-ranging circuit, selects either an input sample (at TP1), or the output from op-amp (U308, pin 6). The op-amp output has a gain of 8 as compared to the sample at TP1.

The signal selection is determined by an evaluation of the magnitude of the sample at TP1. The sample compares with reference voltages from U307 pin 1 (+0.6V) and U307 pin 7 (-0.6V). If the sample is within 0.6V, the output voltages at U310 pins 1 and 7 will be at high voltage states; the signal with a gain of 8 will be identified by U311, and U300 will make the actual signal selection. If the sample is outside the 0.6V limits, the output voltages at U310 pins 1 and 7 will be at low voltage states, causing U311/U300 to select the signal from TP1. The signal is then converted by the analog-to-digital converter (U303), which is accurate to 12 bits. (The 12-bit A/D converter, plus sign bit and auto-ranging, yields 15 bits resolution of sample values.)

The conversion (at U303) takes place when the signal “CONV” is generated from the Microprocessor (U100) and received at U306. The signal, at U306 pin 13, generates a 1 μs pulse which activates the A/D conversion.

Data from the A/D converter is read by buffers (U304, U305), which are enabled by Programmable Array Logic (PAL, U105) signal “SEL6*”. (**See Schematic, Sheet 1**). PAL decodes the address bus from the Microprocessor (U100) through buffers (U101, U102). (The double lines on Schematic, Sheet 1 means 16 lines in parallel.)

NOTE: The asterisk (*) shown in this segment, as in SEL6*, means that the line (logic) is normally high (logic 1 state).

For normal program executions, PAL signal SEL0* is low to fetch the program instructions stored in the

EPROMs (U103, U104). Each EPROM contains up to 32,000 bytes of information.

The Random-Access-Memory (RAM) chips (U200, U201) provide 32K x 8 working space for read, write and data storage by the Microprocessor (U100). If the address lines 13 and 15 are high it causes SEL1* to go low); then the RAM chips can be accessed by the PAL chip (U105).

A nonvolatile RAM (NOVRAM) chip (U202) is used for storing settings and targets (fault data) when the relay is deenergized. All information is stored in the NOVRAM in three places for reliability and security purposes. If there is a discrepancy between all three information entries, the Alarm-1 relay will "drop out", and the Relay In Service LED (RS2) will be turned "OFF". If two of three are identical, the information will be displayed, and the third position will be updated. If the third position fails to restore and match the other two positions, the relay continues to operate, and shows self-check (bit 1) in the test mode.

In order to access the NOVRAM, if address lines 12, 13 and 15 (of U105) go high it will cause signal SEL2* to go low.

If address lines 14 and 15 go high, it will make SEL3* go low. The microprocessor (U100) transfers and updates the information to the Display module LEDs (on the front panel), and vacuum fluorescent display, through buffers (U203, U204).

If address lines 11, 14 and 15 (of U105) go high, the signal SEL4* will go low. This enables the buffers (U205 and U206) for the Front Panel Switch Inputs; the Microprocessor also acknowledges the status of the output reed relays which monitor the "trip" current flow.

If address lines 12, 14 and 15 (of U105) go high, the signal SEL5* will go low; the selected output relays and alarm relays will be addressed. Since buffers (U207, U209), for the Relay Control Signals, are octal three state D type flip flop, the relays will stay "ON" until the Microprocessor resets the outputs. SEL5* also selects the input channel of the multiplexer, through MUX signals (MUX1, MUX2, and MUX4).

If address lines 11, 12, 14 and 15 (of U105) go high, the signal SEL6* will go low; the digital numbers from analog measurement are transferred to memory (EPROM) thru buffers (U304, U305)...(**see Schematic, Sheet 2**).

If address lines 13, 14 and 15 (of U105) go high, the signal SEL7* will go low; the clock setting and clock reading are enabled.

The Microprocessor (U100) performs logic operations, calculates data from the A/D converter, and makes decisions (e.g., when to energize the output relays). It also receives the following digital I/O signals directly from the opto coupler (on the Interconnect module):

- Ext. Reset
- 52b
- 52a
- RCVR #1
- RCVR #2
- PLT ENA
- SPB (89b)
- (not used)

Microprocessor port #1 (P1) is used for INCOM communications. Five lines (DATA, SCK, R/W*, INT, and BUSY*) are compatible with any INCOM/PONI boxes (**see Interconnect Module**).

A series voltage regulator (U500), **see Schematic, Sheet 2**) regulates +5V for all power supply logic. Input power failure is detected by Q501 and Q502 thru Z500 Signal PFAILl* (from Q501) is normally high. If the 8.5V power supply drops to 7V, Q502 will turn "OFF"; Q501 will turn "ON" and the PFAIL* signal drops from high to low. This action resets the Microprocessor and blocks all output relays contingent upon U106 (pin 11 and Q100).

The +5V and -6.8V power supplies are also fed to A/D converter thru U300. At normal condition, the Power Supply Monitor enable (PSME) arms the trip output gates. If any P/S failure is detected, the PSME (software) will disable the trip action.

The Microprocessor module includes the following jumpers:

JUMPER	POSITION	FUNCTION
JMP1	1-2	EEPROM (8K x 8)
JMP2	1-2	Programmable Contacts or Three-pole Trip
	2-3	Single-Pole Trip Option
JMP3	OUT	Phase Rotation ABC
	IN	Phase Rotation ACB
JMP4	IN	Dropout Time Delay (0/50) For Trip
	OUT	No Dropout Time Delay
JMP5	IN	Enable Output Contact Test
	OUT	Disable Output Contact Test
JMP6	IN	A/D Calibration Mode
	OUT	Normal
JMP7		Not used
JMP8,9	1-2	RAM (32K x 8)
JMP 10,11, and 12		Spare

NOTE: When the MDAR is being calibrated, move the jumper from JMP12 to JMP6 position. After calibration, replace the jumper back at the JMP12 position.

Three trimpots (R301, R303, R405) are used to calibrate the A/D converter; a variable capacitor (C504) is used for clock adjustment (**see Schematic, Sheet 2**). The MDAR relay has been properly adjusted at the factory; adjustments by the customer are not required. The following Factory calibration procedure is for reference only.

1. Turn “OFF” all Vac and Vdc power.

2. Remove the inner chassis from the outer chassis, by using a screw driver at the front panel.

3. Connect together all terminals on J11 (from J11-1A to J11-7A, and J11-1C to J11-7C) thru an external mating connector.

4. Move jumper from JMP12 to JMP6.

5. Remove U404 (Sample/Hold device) from its socket (**see Schematic Sheet 2**).

6. Connect a digital voltmeter (with at least 5 digits) to TP3, and TP2 (common).

7. Using a battery and potentiometer, connect the adjustable voltage to TP1, and common to TP2. (Apply voltage per steps 11 and 12.)

8. Apply a rated dc voltage across the two fuses of the Interconnect PC Board, and turn “ON” the dc power source (**see Power Supply module**).

9. On the front panel, depress the Display Select push-button until the TEST LED is illuminated.

10. Raise the Function field display to “ADC’ mode. The Value field display shows the average Hex value of the analog input over one cycle.

11. Set the Voltmeter input to - 4.99878 Vdc. Adjust Pot R303 until the Value display reads C009 (**see A/D Converter offset adjustment**).

12. Set the voltmeter input to +4.99634 Vdc. Adjust pot R301 until the Value display reads 3FF4. (**See A/D Converter Gain adjustment**.)

13. Turn “OFF” the dc Power Supply.

14. Remove the battery voltage from TP1 and TP2.

15. Remove the digital voltmeter.

16. Replace U404 into its socket.

17. Turn “ON” the dc power supply and adjust pot R405 until the Value display reads 0 or FFFF. (**See Sample/Hold, U404 offset adjustment**.)

NOTE: The value “FFFF” is a hexadecimal number.

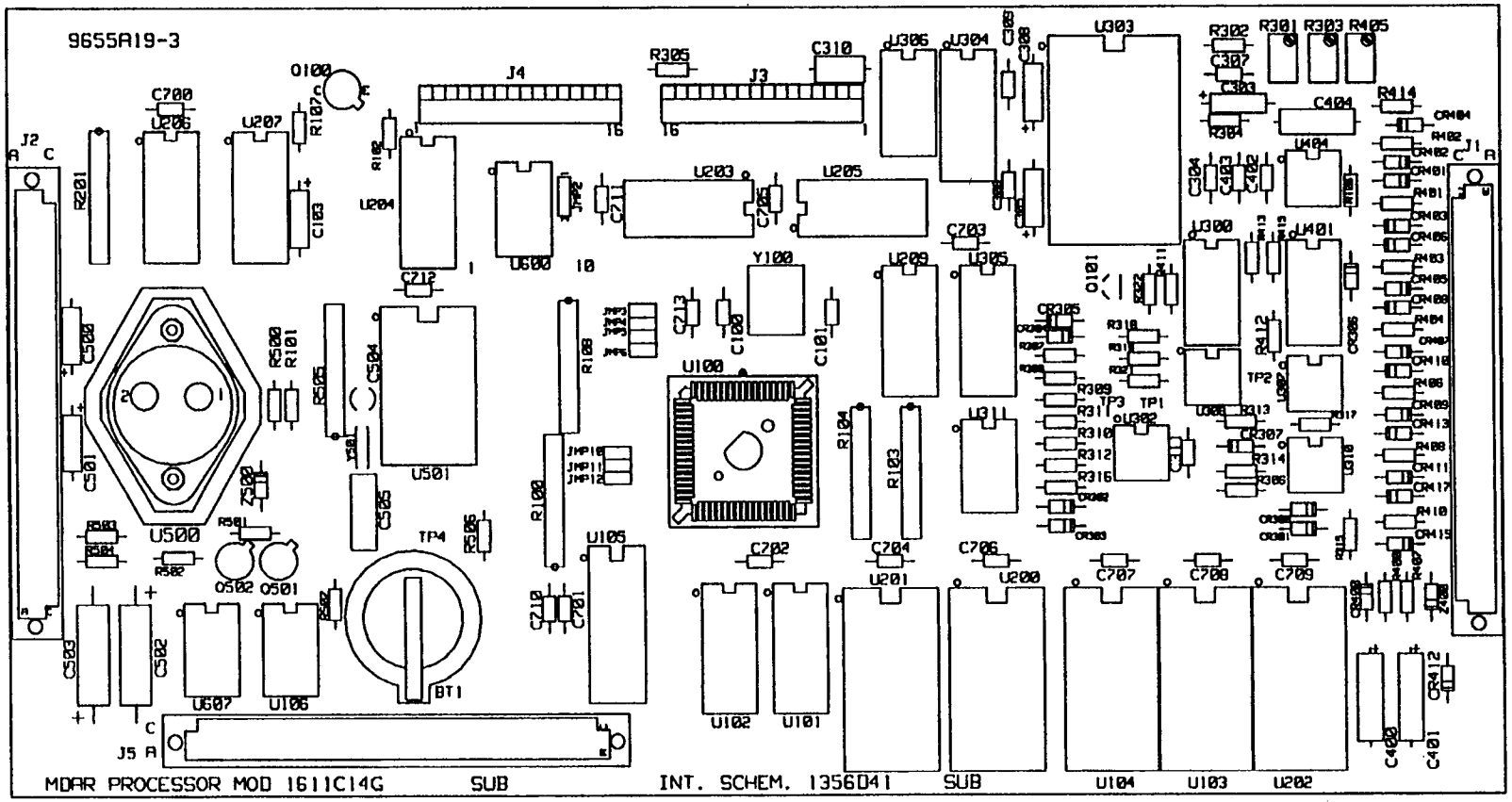
18. Connect a precision period/counter instrument to TP4 and TP2 (common). Adjust variable capacitor (C504) to read the period of pulses at TP4. It should be 1 .000000 second (0 .000002).

19. Turn “OFF” the dc power supply.

20. Remove the power leads and external connector (J11).

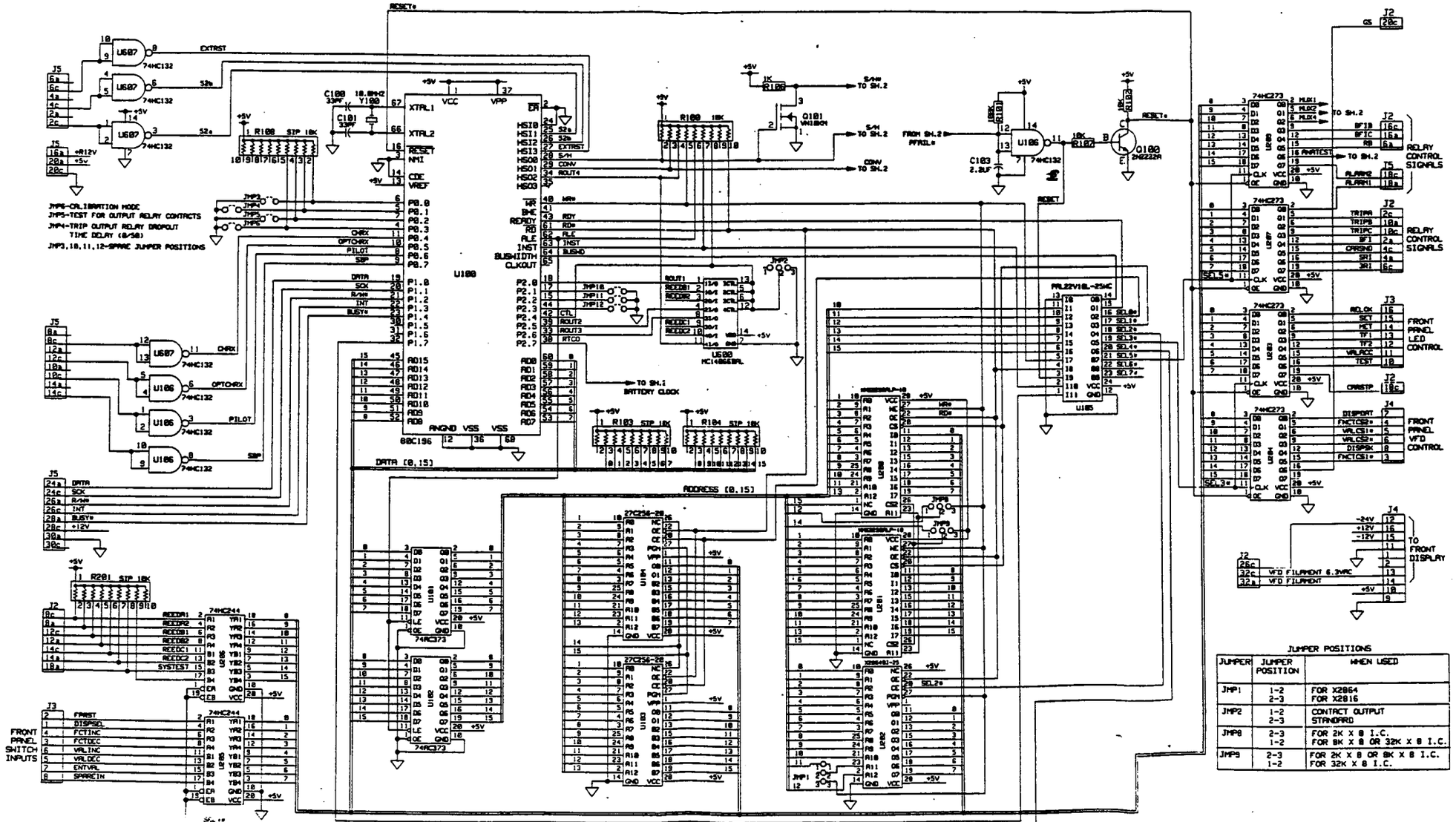
21.Move jumper from JMP6 to JMP12 position.

22. Slide the inner chassis into the outer chassis and lock the outer chassis with a screw driver.



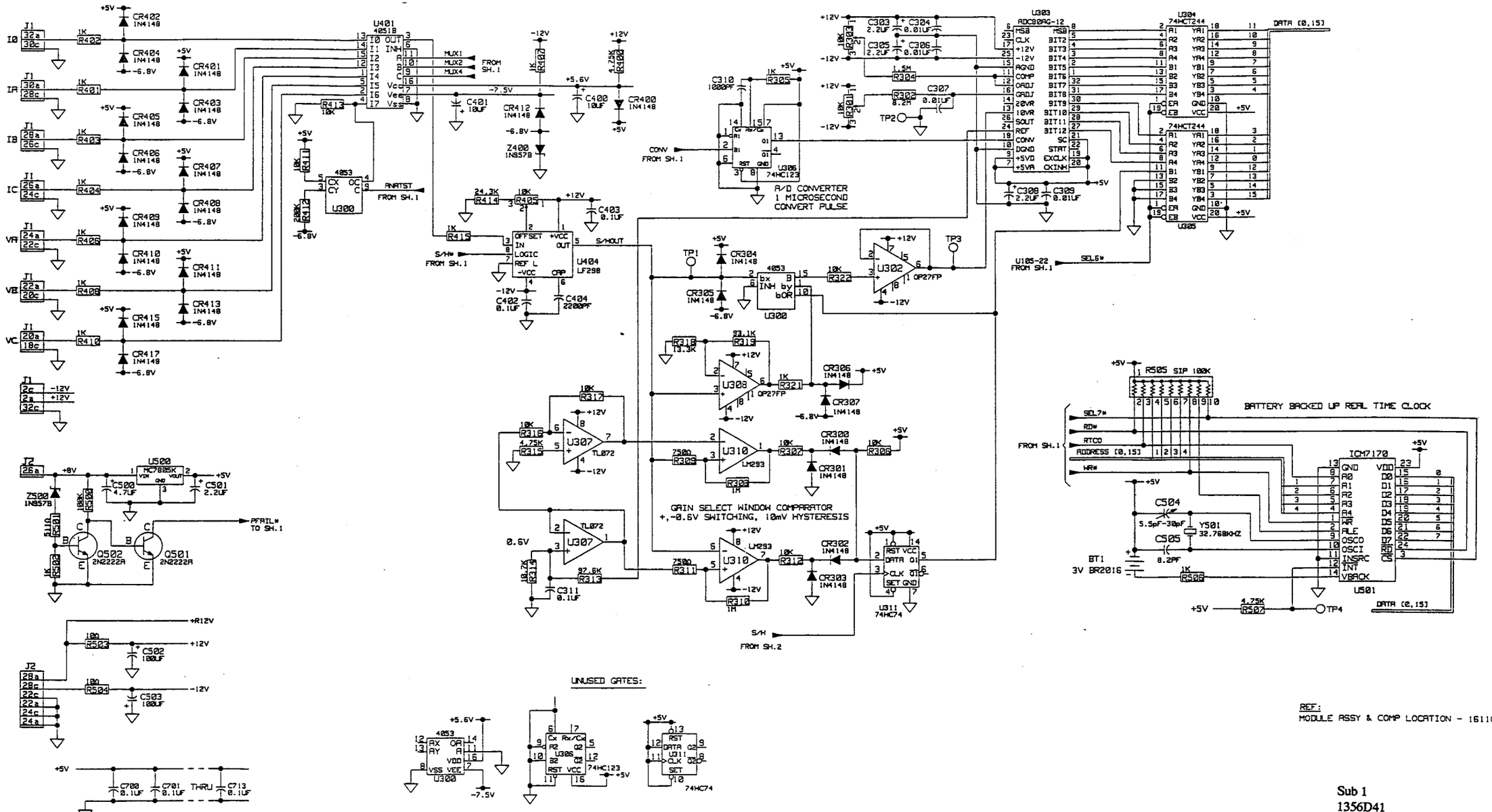
Sub 5
1611C14
Sheet 5 of 5

Figure E-1 MDAR Microprocessor Component Location Diagram.



Sub 1
1356D41

Figure E-2. MDAR Microprocessor Module Schematic



Sub 1
1356D41
Sheet 2 of 2

(3/92)

Figure E-2. MDAR Microprocessor Module Schematic

MDAR MICROPROCESSOR MODULE 1611C14 SUB 10

COMP	DESCRIPTION	STYLE	GROUP
BATTERIES			
BT1	3V 75MA BR-2016	9648A03H01	21, 23
CAPACITORS			
C300, 301	33PF 100V 10% CERAMIC	CQ330AKLD4	21, 23
C304, 306, 307, 309	.01MFD 50V 10% CERAMIC	CB1002KH77	21, 23
C103, 303, 305, 308, 501	2.2MD 35V 5%	CJ2204JGA2	21, 23
C310	1000 PF 5% 200V MET POLYCARB	CF1001JP78	21, 23
C311, 402, 403, 700 to 713	.1MFD 50V 10% CERAMIC	CB1003KH77	21, 23
C400, 401	10 MFD 20% 20V TANTALUM	CJ1005MD06	21, 23
C404	2200 PF +/-5% 100V	CG2201JLC8	21, 23
C500	4.7 UF 20% 20V MOLDED TANTALUM	CJ4704MD72	21, 23
C502,503	100 UF 20% 35V TANTALUM	CJ1006MGC4	21, 23
C505	8.2 PF 2% 500V DIPPED MICA	CR820BGV92	21, 23
C700 thru C713	0.1 UF +/-10% 50-59V CERAMIC	CB1003KH77	21, 23
CONNECTORS			
J1, J2, J5	32 PIN DIN CONNECTOR 100-032-432	9646A11H03	21, 23
J3, J4	1000-216-2105	3532A99H11	21, 23
CRYSTALS			
Y100	10MHZ 18PF 25-OHM	879A920H11	21, 23
Y501	32.768 KHZ STATEX CX-1V	9649A33H01	21, 23
INT CKT			
U100	TN80C196KB-12	1499B02H01	21,23
U101. 102	OCTAL LATCH CD74RC373E	9650A22H01	21, 23
U103	27C256-20 EPROM	1499B06G11	21, 23
U105	PALC22V10L-25WC	1502B45G02	21, 23
U106, 607	QUAD NAND SCHMITT 74HC132N	9656A02H01	21, 23
U203, U204, & U207, U209	MC74HC273N OCTAL D-TYPE FLIP-FLOP	9656A03H01	21, 23
U205, 206	74HC244N	9650A44H51	21, 23
U300	MC14053BCP	3533A70H01	21, 23
U302, 308	ULTRA LOW NOISE OP-AMP OP-27FP	3533A97H01	21, 23
U303	12 BIT A/D ADC80AG-12	9561A72H01	21, 23
U304, 305	OCTAL DRIVER 74HCT244E	9652A49H06	21, 23
U306	ONE SHOT MULTIVIEATOR 74HC123E	9450A23H51	21, 23
U307	TL072IJ DUAL J-FET INPUT OP-AMP	3528A90H02	21, 23
U310	LM293N DUAL COMPARATOR	9647A06H01	21, 23
U311	DUAL D FLIP-FLOP 74HC74N	9650A33H62	21, 23
U401	MC14051BAL 8-CHAN MUX	9447A67H52	21, 23
U404	LF298FE	9649A97H01	21, 23
U500	LAS15A05	775B891H01	21, 23
U501	ICM7170AIPG REAL-TIME CLOCK	9649A92H01	21, 23
U600	MC14066BAL	3527A09H06	21, 23
DIODES			
CR300 to 307 & CR400 to 417	1N4148 75V 0.01A	836A928H06	21, 23

COMP	DESCRIPTION		GROUP
EPROMS			
U103	27C256-20 EPROM (V2.1X	1499B06G11	
U104	27C256-20 EPROM (2.1X	1499B06G12	
U202	Pilot, Single-Pole Trip	1502B22G32	52
U202	Pilot, Three-Pole Trip or Programmable Output Contacts	1502B22G33	53
U202	Non-Pilot Single-Pole Trip	1502B22G35	55
U202	Non-Pilot Trip or Programmable Output Contacts	1502B22G36	56
IC SOCKETS			
U303	32 PIN	9649A94H01	23
INT CKTS			
U303	ADC 80AG-12 A/D CONVERTER	9651A72H01	23
LINEAR ICS			
U307	TLO72IJ DUAL OP-AMP	3528A90H02	23
U308	OP27GZ SINGLE OP-AMP (LO NOISE)	3533A97H01	23
U310	LM293P DUAL COMPARATOR	9647A06H01	23
U404	LF298FE SAMPLE AND HOLD	9649A97H01	23
U500	LAS15A05 POS VOLTREG 15V 2% 1.5A	775B891H01	23
MEMORYS			
U200	KM62256 ALP-10 RAM-CMOS	9649A96H02	
U201	KM62256 ALP-10 RAM-CMOS	9649A96H02	
MICROPROCS			
U100	TN80C196KB-12 MICROCONTROLLER	1499B02H01	23
PALS			
U105	PAL	1502B45G01	23
POTENTIOS			
R301	10K 25T TOP ADJ	3534A25H07	23
R303	10K 25T TOP ADJ	3534A25H07	23
R405	10K 25T TOP ADJ	3534A25H07	23
RES NETS			
R100 9	COMM TERML 10 KILOHMS 2% SIP	3532A91H03	23
R103 9	COMM TERML 10 KILOHMS 2% SIP	3532A91H03	23
R104 9	COMM TERML 10 KILOHMS 2% SIP	3532A91H03	23
R108 9	COMM TERML 10 KILOHMS 2% SIP	3532A91H03	23
R201 9	COMM TERML 10 KILOHMS 2% SIP	3532A91H03	23
R505 9	COMM TERML 100 KILOHMS 2% SIP	3532A91H06	23
RESISTORS			
R101	100 KILOHMS 1% 0.25W METAL FILM	RM1003FQ98	23
R102	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R106	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R107	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R302	8.2 MEGOHMS 5% 0.25W CARBON FILM	RB8204JQB3	23
R304	1.50 MEGOHMS 1% 0.25W METAL FILM	RM1504FQ99	23
R305	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R306	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R307	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23

COMP	DESCRIPTION		GROUP
R308	1.00 MEGOHMS 1% 0.25W METAL FILM	RM1004FQ99	23
R309	750 OHMS 1% 0.25W METAL FILM	RM7500FQB1	23
R310	1.00 MEGOHMS 1% 0.25W METAL FILM	RM1004FQ99	23
R311	750 OHMS 1% 0.25W METAL FILM	RM7500FQB1	23
R312	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R313	97.6 KILOHMS 1% 0.25W METAL FILM	RM9762FQA9	23
R314	10.7 KILOHMS 1% 0.25W METAL FILM	RM1072FQA9	23
R315	4.75 KILOHMS 1% 0.25W METAL FILM	RM4751FQB0	23
R316	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R317	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R318	13.3 KILOHMS 0.1% 0.125W METAL FILM	RM1332CE63	23
R319	93.1 KILOHMS 0.1% 0.125W METAL FILM	RM9312CE63	23
R321	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R322	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R400	4.75 KILOHMS 1% 0.25W METAL FILM	RM4751FQB0	23
R401	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R402	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R403	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R404	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R406	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R407	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R408	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R410	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R411	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R412	200 KILOHMS 1% 0.25W METAL FILM	RM2003FQ98	23
R413	10.0 KILOHMS 1% 0.25W METAL FILM	RM1002FQA9	23
R414	24.3 KILOHMS 1% 0.25W METAL FILM	RM2432FQA9	23
R415	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R500	100 KILOHMS 1% 0.25W METAL FILM	RM1003FQ98	23
R501	511 OHMS 1% 0.25W METAL FILM	RM5110FQB1	23
R502	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R503	10.0 OHMS 1% 0.25W METAL FILM	RM100AFQB4	23
R504	10.0 OHMS 1% 0.25W METAL FILM	RM100AFQB4	23
R506	1.00 KILOHMS 1% 0.25W METAL FILM	RM1001FQB0	23
R507	4.75 KILOHMS 1% 0.25W METAL FILM	RM4751FQB0	23
SOCKETS			
I105	2-641933-1 24PIN	1479B86H06	23
U100	821574-1 68 PIN PLCC AMP	9649A91H01	23
U101	20 PIN DIP	1479B86H04	23
U102	20 PIN DIP	1479B86H04	23
U103	28 PIN	1479B86H05	23
U104	28 PIN	1479B86H05	23
U200	28 PIN	1479B86H05	23
U201	28 PIN	1479B86H05	23
U202	28 PIN	1479B86H05	23
U203	20 PIN DIP	1479B86H04	23
U204	20 PIN DIP	1479B86H04	23
U205	20 PIN DIP	1479B86H04	23
U207	20 PIN DIP	1479B86H04	23
U208	14 PIN IC SOCKET	774B996H01	23

COMP	DESCRIPTION		GROUP
U209	20 PIN DIP	1479B86H04	23
U300	16 PIN IC SOCKET	774B996H03	23
U302	8 PIN IC SOCKET	774B996H02	23
U303	8 PIN IC SOCKET	774B996H02	23
U304	20 PIN DIP	1479B86H04	23
U305	20 PIN DIP	1479B86H04	23
U306	16 PIN IC SOCKET	774B996H03	23
U307	8 PIN IC SOCKET	774B996H02	23
U310	8 PIN IC SOCKET	774B996H02	23
U401	16 PIN IC SOCKET	774B996H03	23
U404	8 PIN IC SOCKET	774B996H02	23
U501	24 PIN	1479B86H02	23
U700	14 PIN IC SOCKET	774B996H01	23
U702	14 PIN IC SOCKET	774B996H01	23
U703	14 PIN IC SOCKET	774B996H01	23
TERMINALS			
TP1, 2, 3, 4	TEST PIN	880A937H01	21, 23
TRANSISTORS			
Q100, 501, 502	N2222A 40V 0.8A 0.4W NPN	762A672H15	21, 23
Q101	VN10KM	9641A07H06	21, 23
TRIM CAPS			
C504	***NO ITEM DESCRIPTION***	3516A79H01	23
ZENERS			
Z400, Z500	1N957B 6.8V 5% 0.4W	186A797H06	23

Appendix F. DISPLAY MODULE

The Display module contains a blue vacuum fluorescent alphanumeric display, with 4 characters in the function field and 4 characters in the value field; it also includes 7 LEDs, 7 push-button switches and 5 test points (**See Figures 1-1, F-1** and Schematic). The 7 push-button switches (SW1 thru SW7) are used to activate the following functions on the front panel:

- Display Select (the LEDs, to the right of this push-button, indicate the selected function)
- Reset (the targets selected)
- Function Raise (move to the following function)
- Function Lower (move to the previous function)
- Value Raise (move to the next higher value)
- Value Lower (move to the next lower value)
- Enter (the value that has been selected for upper contact testing)

The Microprocessor module scans these switches once every cycle while in the “background” mode, where it looks for phase current or phase voltage disturbances. When a phase disturbance is detected, the relay enters the “fault” mode. While scanning, the Microprocessor module updates the Display module via the ICs (U1, U2, U3 and U4). The display will be blocked momentarily once every minute due to the self-check function. This is for readout check and will not interrupt the relay protection function. The Microprocessor also illuminates some LEDs when the Display Select Switch is depressed. IC (U5) controls the LEDs, which are as follows (**see Section 1.3.6**):

- Relay In Service (DS2)
- Settings (DS3)
- V/I/Angle (DS4)
- Last Fault (DS5)
- Previous Fault (DS6)
- Value Accepted (DS7)
- Test (DS8)

Test points (TP1 thru TP5) are used to monitor dc voltages; these voltages can be measured from the front panel, as follows:

- -24V (TP1)
- + 5V (TP2)
- -12V (TP3)
- +12V (TP4)
- Common (TP5)

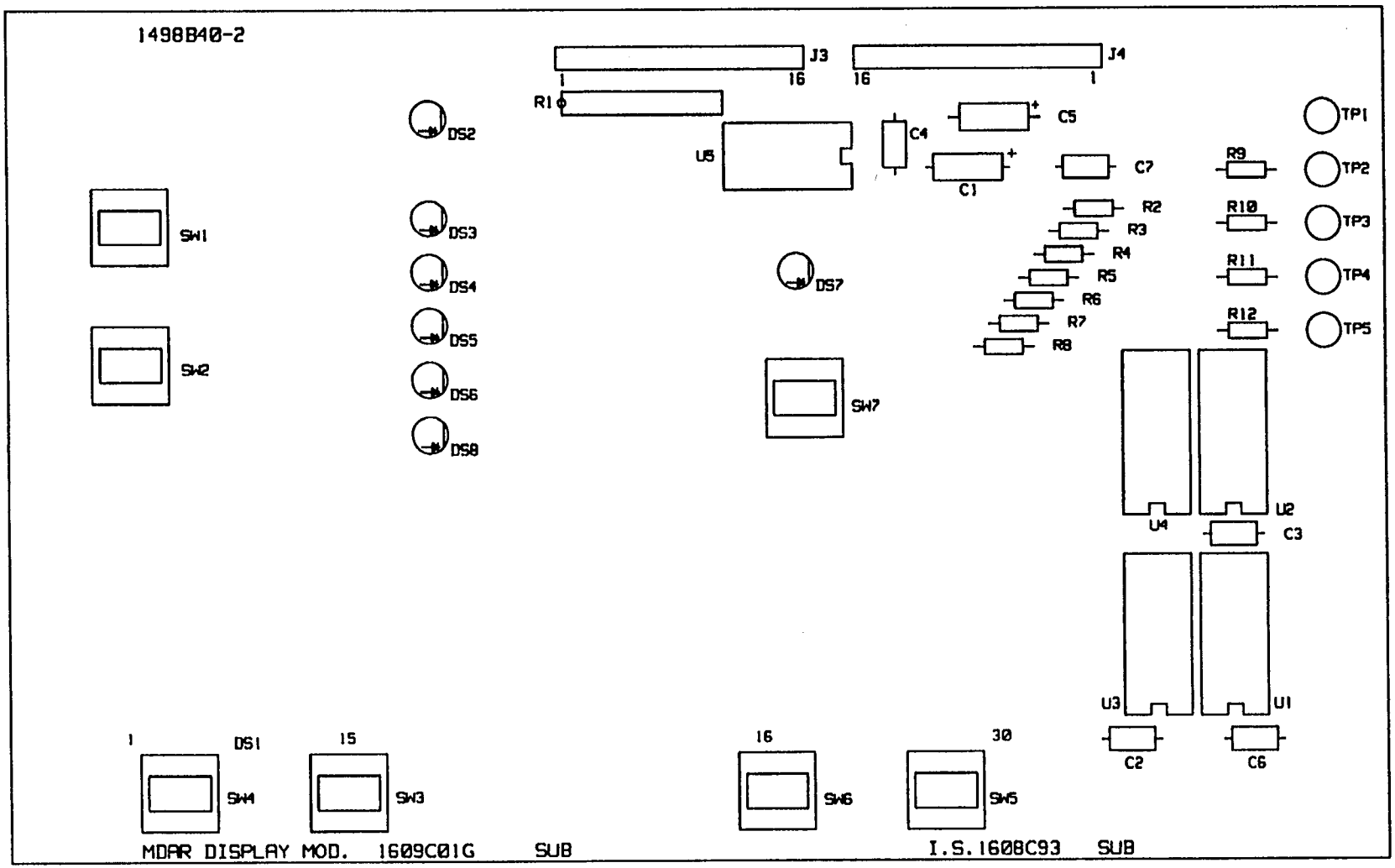


Figure F-1 MDAR Display Module PC Board.

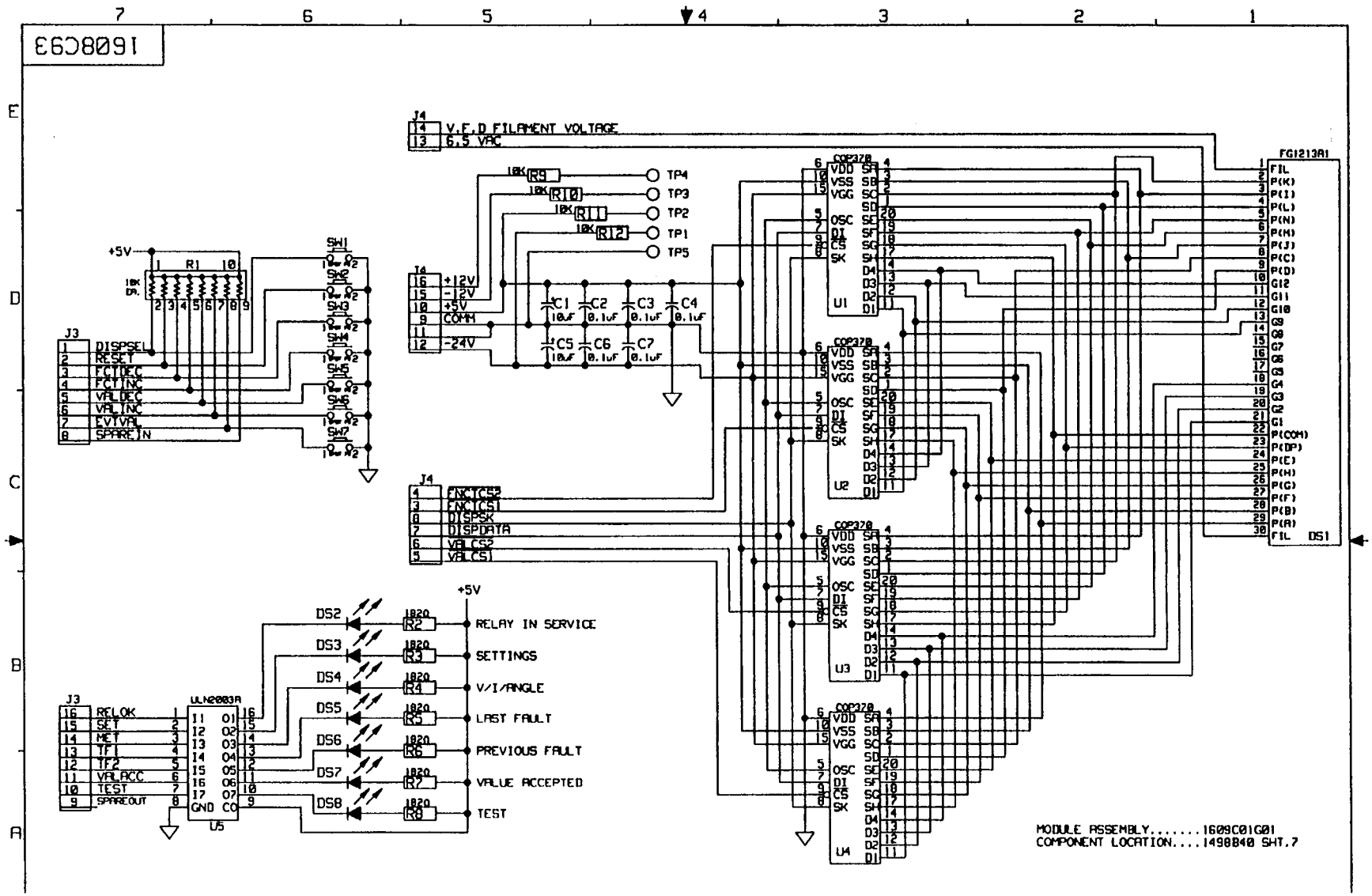


Figure F-2 MDAR Display Module Schematic.

Sub 1
1608C93

MDAR DISPLAY MODULE 1609C01	SUB 4	6/4/92	
PC BOARD	SUB 1	1498B40	01

COMP LOC	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1	10uf 20V	184A661H24	01
C2, 3, 4, 6, 7	0.1uf 50V	3534A26H05	01
C5	10uf 35V	862A530H15	01
CONNECTORS			
J3, 4	16 PIN HEADER	3534A19H14	01
DISPLAYS			
DS1	FG1213A1	1498B48H01	01
LEDS			
DS2, 8	LED YELLOW	3532A41H04	01
DS3, 5, 6	LED RED	3532A41H01	01
DS4, 7	LED GREEN	3532A41H03	01
INT CKT			
U1, 2, 3, 4	COP370	9645A02H01	01
U5	ULN-2003	3533A01H01	01
RES NETS			
R1	10K SIP 9X	3532A91H03	01
RESISTORS			
R2, 3, 4, 5, 6, 7, 8	182Ω .25W 1%	3535A39H26	01
R9, 10, 11, 12	10K .25W 1%	3535A37H01	01
SOCKETS			
U1, 2, 3, 4	20 PIN	1479B86H04	01
U5	16 PIN	3534A76H04	01
SWITCHES			
SW1, 2, 3, 4, 5, 6		9645A08H02	01
SW7		9645A08H01	01
TERMINALS			
TP1, 2, 3, 4, 5		849A242H01	01

Appendix G. POWER SUPPLY MODULE

Schematic 1355D07-10
PC Board 1497B66-9
Parts List 1608C35-16

The Power Supply module (**see Figure G-1 and Schematic**) is available in three ranges:

- 38 - 70 Vdc
- 88 - 145 Vdc
- 176 - 290 Vdc

It operates with an isolated dc/dc converter. The secondary windings of the step-down Transformer (T1) supply the following voltages to MDAR modules:

- +12 Vdc
- -12 Vdc
- -24 Vdc
- +24 Vdc
- +8.5 Vdc
- 6.5 Vac (square wave)

The analog amplifiers, A/D converter and alarm relays use13 Vdc. The vacuum fluorescent display uses -24 Vdc and 6.5 Vac. The 24 Vdc is for the INCOM power supply. All logic and Microprocessor related circuits use +5 Vdc which is generated from the +8.5 Vdc supply.

Twelve relays are used for the pilot system. The relay functions are as follows:

- Reed relays for monitoring 2 different breaker currents
- Telephone relays for phase A tripping
- 1 Telephone relay for single pole reclose initiate
- 1 Telephone relay for three pole reclose initiate
- 1 Telephone relay for reclose block
- 1 Telephone relay for breaker failure initiate
- 1 Telephone relay for system test
- 1 Reed relay for general start
- 1 Reed relay for carrier send
- 1 Reed relay for carrier stop

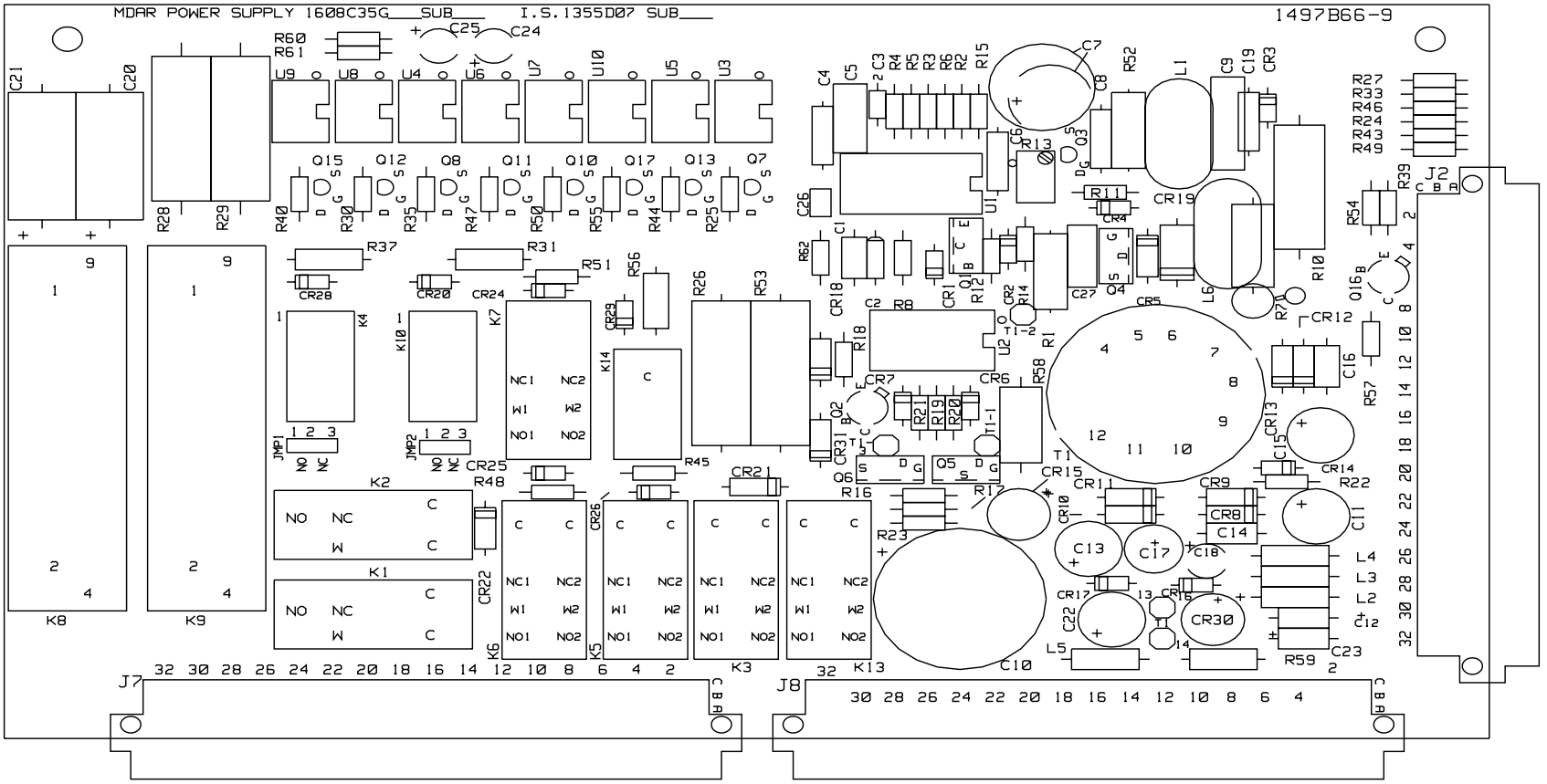
NOTE: Check JMP1 & JMP2 positions for normally open or close output contacts of the carrier SEND and STOP. This note applies to module Sub 13 and higher.

The dc power supply on terminal J8 (22A, 22C) is fed from the Interconnect module (terminals 13 and 14 of 1FT-14, thru two fuses).The full-wave rectifier (CR15) provides a positive voltage at C10, regardless of the input voltage polarity. Transistor (Q1) supplies the initial start voltage to the pulse-width modulated regulator (U1), which is oscillated at approximately 20 kHz (as determined by the values of R4 and C3).

A signal from U1 pin 3 pulses the dual flip-flop (U2), driving Q5 and Q6 to provide a square wave at Transformer (T1).This Transformer has a ferrite pot core that provides the output voltages: 13 Vdc, -24 Vdc, +8.5 Vdc, and 6.5 Vac square wave. The amplitudes of the output voltages can be adjusted by trimpot (R13).The regulator (U1) pins 1 and 2 are used as a comparator to determine the pulse-width at pin 13; this controls the conducting time of series regulator (Q4).Overcurrent shutdown is prevented by R16, R17, R23 connected in parallel. A voltage drop >200mV across these resistors starts the current-limiting circuitry of U1.

Output relays (K1 thru K10 and K14) are logically energized by the Microprocessor (U100) through an optical-isolated coupler (e.g. U8 for K1, K2). All relay driver circuits are similar in design. The following discussion gives an example of the trip circuit (TRIPA-1). A 5 Vdc input from the Microprocessor (U100) will turn on U8 and Q12 (for TRIPA-1) which energizes trip relays (K1, K2).The pickup time of K1, K2 is improved by components R28, R29, C20, C21.Two reed relays (K8, K9) are used for monitoring the breaker trip current. As soon as the trip current is detected, the contacts of K8 and/or K9 will close to send a message to the Microprocessor to begin storing fault data into its memory. The telephone type relay (K13) has two normally-open contacts. For normal operation, VBFI is shorted to B+ through the external jumper between terminals 13 and 14 of 2FT-14, (behind the relay); hence, K13 is energized. Power supply source +43V will be applied to K5 and

K6, through one set of contacts (K-13, 3/4); the signal thru the second set of contacts (K-13, 7/8) is fed to the Microprocessor. Regardless of whether Q11 or Q13 is “ON” or “OFF” when switch 13 of 2FT-14 is opened, K13 will deenergize; then the single pole and three pole reclose contacts are blocked.



* Sub 9
1497B66

Figure G-1. MDAR Power Supply PC Board.

* Denotes Change

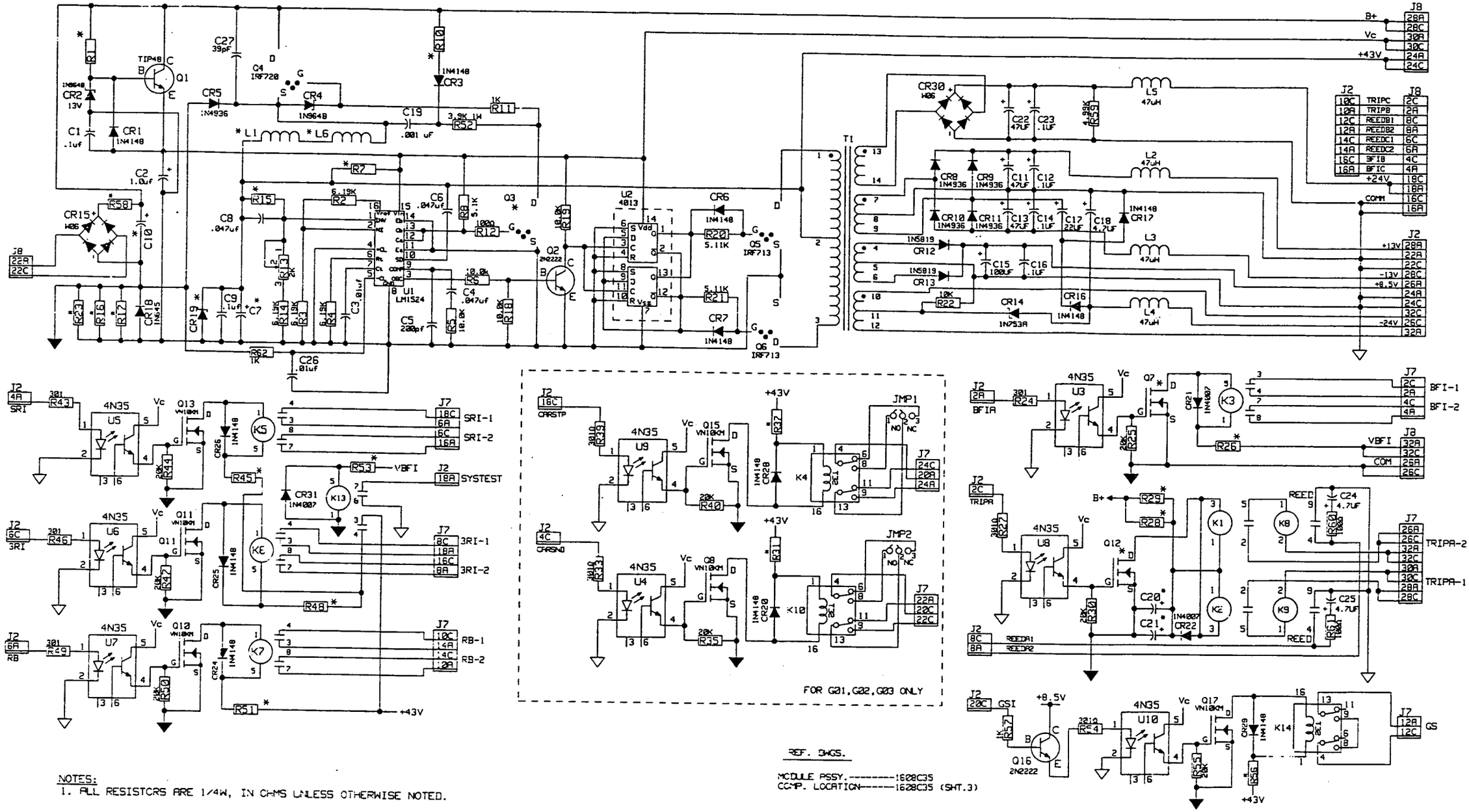


Figure G-2. MDAR Power Supply Schematic

MDAR POWER SUPPLY MODULE 1608C35 SUB 16

48V PILOT		G01
125V PILOT		G02
250V PILOT		G03
48V NON-PILOT		G04
125V NON-PILOT		G05
250V NON-PILOT		G06
PC BOARD SUB 9	1497B66	ALL

COMP LOC	DESCRIPTION	STYLE	GROUP
CAPACITORS			
C1, 12, 14, 16, 23	0.1 uF 50V 10% CER	3534A26H05	01,2,3,4,5,6
C2	1.0 uF 35V TANTALUM	862A530H06	01,2,3,4,5,6
C3	0.01 uF 50V 10% CER	3534A26H04	01,2,3,4,5,6
C4, 6, 8	0.047 uF 100V,+-5% MET-POLY CARB	3534A68H07	01,2,3,4,5,6
C5	200pF 500V,+-2% DUR-MICA	762A757H11	01,2,3,4,5,6
C7	100 uF 100V -10 + 100% AL-ELEC	9645A13H11	02,3,5,6
C7	470 uF 50V 20% AL-ELEC	9645A36H02	01,4
C9	0.1 uF 100V 5% MET-POLY	184A663H04	01,2,3,4,5,6
C10	150 uF 200V 20% AL-ELEC	9647A29H01	02,5
C10	220 uF 160V 20% AL-ELEC	9647A29H02	01,4
C10	47 uF 400V 20% AL-ELEC	9647A29H03	03,6
C11, 13, 22	47 uF 35V -10 +100% AL ELEC	9645A13H02	01,2,3,4,5,6
C15	100 uF 20V -10 + 100% AL-ELEC	9641A08H01	01,2,3,4,5,6
C17	22 uF 35V, 20% DIPPED TANT.	3533A75H11	01,2,3,4,5,6
C18, 24, 25	4.7 uF 50V +20% TANTALUM	3533A75H02	01,2,3,4,5,6
C19	0.001 uF, 200V, +-5% MET-POLY CARB	3534A68H02	01,2,3,4,5,6
C20, 21	1.0 uF 200V FLAT MET-MYLAR	876A409H10	01,2,4,5
C20, 21	0.47 uF 400V	878A531H03	03,6
C26	0.01 uF, 50V	CP1002MH65	01,2,3,4,5,6
C27	39 PF .2%	CR390AGV92	01,2,3,4,5,6
CHOKES			
L1	4MH 350MA EC30HL32	9645A18H02	01,4
L1, 6	16MH 200MA EC30HL35	9645A18H01	02,3,5,6
L2, 3, 4, 5	47UH 10%	9645A17H02	02,3,5,6
L6	16 MH 200MA EC30HL35	9645A18H01	03,06
CONNECTORS			
J2, 7, 8	PD32-10302-100 RIGHT ANGLE DIN CON	9646A11H02	01,2,3,4,5,6
DIODES			
CR1, 3, 6, 7, 16, 17 20, 24, 25, 26, 28, 29	1N4148 75V 10 MILLIAMPS	836A928H06	01,2,3,4,5,6
CR5,8, 9, 10, 11	1N4936 400V 1A	836A928H10	01,2,3,4,5,6
CR12, 13	1N5819 40V1A	9648A05H02	01,2,3,4,5,6
CR14	1n753A	862a606h01	01,2,3,4,5,6
CR15, 30	W06M BRIDGE RECT.	3510A67H01	01,2,3,4,5,6
CR18	1N645A 225V .2 AMP	837A692H03	01,2,3,4,5,6
CR19	51V 5W 5% 1N5369B	862A288H42	02,3,5,6
CR21, 22, 31	RECTIFIER 1A 1000V 1N4007	836A928H08	01,2,3,4,5,6

COMP LOC	DESCRIPTION	STYLE	GROUP
IC SOCKETS			
U1	16 PIN DIP	3534A76H04	01,2,3,4,5,6
U2	14 PIN	3534A76H03	01,2,3,4,5,6
U3, 4, 5, 6, 7, 8, 9, 10	6 PIN IC SOCKET DIP	3534A76H01	01,2,3
U3, 5, 6, 7, 8, 10	6 PIN IC SOCKET DIP	3534A76H01	04,5,6
INT CKTS			
U1	SG1524J PULSE WIDTH MODULATOR	3534A92H03	01,2,3,4,5,6
U2	MC14013BCP TYPE D FLIP-FLOP	3535A12H01	01,2,3,4,5,6
U3, 4, 5, 6, 7, 8, 9, 10	4N35 OPTO-ISO.	774B936H01	01,2,3
U3, 5, 6, 7, 8, 10	4N35 OPTO-ISO.	774B936H01	04,5,6
JUMPERS			
R45, 48, 51	ZERO OHM RESISTOR	862A478H01	02,3,5,6
R45, 48, 51, L6	ZERO OHM RESISTOR	862A478H01	02
R45, 48, 51	ZERO OHM RESISTOR	862A478H01	03
R45,48, 51, L6	ZERO OHM RESISTOR	862A478H01	05
R45, 48, 51	ZERO OHM RESISTOR	862A478H01	06
R58	ZERO OHM RESISTOR	862A478H01	01,4
R58, L6	ZERO OHM RESISTOR	862A478H01	01
R58, L6	ZERO OHM RESISTOR	862A478H01	04
	BLUE CHIP	3532A54H01	01,2,3,4,5,6
POTENTIOS			
R13	2K-OHM TOP ADJ. VAR.	3534A25H05	01,2,3,4,5,6
REED RELAYS			
K8	.5 AMP PICKUP, FORM A	1442C62G01	01,2,3,4,5,6
K9	.5 AMP PICKUP, FORM A	1442C62G01	01,2,3,4,5,6
RELAYS			
K1	SPDT 24V 10A	9645A10H02	02,5
K4, 10, 14	DS2EMDC48	3534A32H04	01,2,3
K8, 9	.5A PICKUP FORM A REED	9645A10H01	01,2,3,4,5,6
K14	DS2EMDC48	3534A32H04	01,2,3,4,5,6
RESISTORS			
R1	15K 0.50W 2% METAL GLAZE	629A531H60	01,4
R1	62K OHM 1W 5% MOLDED COMP	187A643H70	02,5
R1	150K 1W 5% MOLDED COMP	187A643H79	03,6
R2, 3, 4	6.19K .25W 1% METAL FILM	3535A38H77	01,2,3,4,5,6
R5, 6, 18, 19, 22	10K .25W 1% METAL FILM	3535A37H01	01,2,3,4,5,6
R7	1500-OHM 2W 5% MOLDED COMP	185A207H31	02,3,5,6
R7	1.5K 0.50W 2% METAL FILM	629A531H36	01,4
R8, 14, 20, 21	5.11K .25W 1% METAL FILM	3535A38H69	01,2,3,4,5,6
R10	2000-OHM 2W 5% MOLDED COMP	185A207H34	01,4
R10	10K 5W 5% WIRE WOUND	763A129H02	02,5
R10	30K 5W 1% WIRE WOUND	763A130H10	03,6
R11	1K .25W 1% METAL FILM	3535A38H01	01,2,3,4,5,6
R12	100-OHM .25W 1% METAL FILM	3535A39H01	01,2,3,4,5,6
R15	100K .25W 1% METAL FILM	3532A38H01	2,3,5,6
R15	66.5K .25W 1% METAL FILM	3535A37H80	01,4
R16, 17	0.5 OHM .4W 1% WIREWOUND	3534A47H06	01,4

COMP LOC	DESCRIPTION	STYLE	GROUP
R16, 17, 23	1.0-OHM .25W 1% METAL FILM	3537A56H01	02,3,5,6
R22, 23	0.5 OHM .4W 1% WIREWOUND	3534A47H06	01,4
R24, 27, 54	301 OHM .25W 1% METAL FLIM	3535A39H47	01,2,3,4,5,6
R25, 30	20K .25W 1% METAL FILM	3535A37H30	01,2,3,4,5,6
R26, 28, 29	5K 5W 5% WIRE WOUND	763A129H01	02,5
R26, 28, 29	1K 5W 5% WIRE WOUND	763A129H07	01,4
R26, 29	20K 5W 5% WIRE WOUND	763A129H08	03,6
R31, 37	499 OHM .5W 1%	RM4990FHH4	01
R31	1.5 K OHM 0.5W 1%	RM1501FHH4	02,3
R33, 39	301 OHM .25W 1% METAL FLIM	3535A39H47	01,2,3
R35	20K .25W 1% METAL FILM	3535A37H30	01,2,3
R37	1.5 K OHM 0.5W 1%	RM1501FHH4	02,3
R40	20K .25W 1% METAL FILM	3535A37H30	01,2,3
R43, 49	301 OHM .25W 1% METAL FLIM	3535A39H47	ALL
R44, 50	20K .25W 1% METAL FILM	3535A37H30	ALL
R45, 48, 51	267 OHM .5W 1% METAL FILM	848A818H92	01,4
R46	301 OHM .25W 1% METAL FLIM	3535A39H47	ALL
R47, 55	20K .25W 1% METAL FILM	3535A37H30	ALL
R52	3.9K OHM 1W 5%	187A643H41	ALL
R53	5K 5W 5% WIRE WOUND	763A129H01	02,5
R53	1K 5W 5% WIRE WOUND	763A129H07	01,4
R53	20K 5W 5% WIRE WOUND	763A129H08	03,6
R56	499 OHM .5W 1%	RM4990FHH4	01,4
R56	1.5K, 0.50W 1%	RM1501FHH4	02,3,5,6
R57, 62	1K .25W 1% METAL FILM	3535A38H01	01, 2,3,4,5,6
R58	15-OHM 3W 5% WIRE WOUND	763A127H36	02,5
R58	25 OHM 3W 5% WIREWOUND	763A127H31	03,6
R59	4.99K 1/2W 1% METAL FILM	848A820H16	01, 2,3,4,5,6
R60, 61	100 OHM .25W 1% METAL FILM	3535A39H01	01, 2,3,4,5,6
TRANSFORMERS			
T1	PS TRANSF	1604C87G05	02,3,5,6
T1	PS TRANSF	1604C87G06	01,4
TRANSISTORS			
Q1	T1P48	861A634H02	01, 2,3,4,5,6
Q2, 16	2N2222A, NPN 40V .8A .4W	762A672H15	01, 2,3,4,5,6
Q3, 7, 12	ZVN0535A	9646A90H01	03,6
Q4	1RF720 400V 2.5A N-MOSFET	9641A07H01	01,2,3,4,5,6
Q5, 6	1RF713 350V 0.9A N MOSFET	9641A07H02	01, 2,3,4,5,6
Q8, 10, 11, 13, 15, 17	VN10KM N-MOSFET	9641A07H06	01,2,3
Q10, 11, 13, 17	VN10KM N-MOSFET	9641A07H06	04,5,6
ZENERS			
CR2, 4	1N964B 13V 5% 400MW	862a606H16	01, 2,3,4,5,6
CR14	1N753A 6.2V 5% 400MW	862A606H01	01, 2,3,4,5,6
CR19	1N5365 36V 5W 5%	862A288H38	01,4
UNREFERENCED ITEMS			
	ROLL PIN	9644A92H01	01, 2,3,4,5,6
	SCREW 4-40 x .188 BIN HDSTL	877A482H02	01, 2,3,4,5,6
	NUT 4-40 HEX STD STL	877A227H04	01, 2,3,4,5,6
	HEAT SINK	3534A17H05	01, 2,3,4,5,6

Appendix H-1. FULL PERFORMANCE TESTS (V2.10)

'The following kinds and quantities of test equipment are used for the MDAR Acceptance Tests:

- Voltmeter (1)
- Ammeter (1)
- Phase Angle Meter (1)
- Load Bank (2)
- Variac (3)
- Phase Shifter (1)
- Optional Doble or Multi-Amp Test System

NOTE: Before turning on the dc power supply, check jumper positions on the Interconnect and Microprocessor modules as shown in Table 4-4. Also, refer to this table for relay system operation.

WARNING

Check jumper #3 on the Microprocessor module is for the selection of phase sequence rotation ABC or ACB. Remove Jumper 3 for system ABC rotation for the following test. Refer to Section 1.8 for ACB system.

Refer to the NOTE under Table H-1 for 1 amp ct application.

1. FULL PERFORMANCE TESTS

Full performance tests explore MDAR responses and characteristics for engineering evaluation. They are in two parts: Non-Pilot and Pilot Acceptance Tests.

NOTE: Customers who are familiar with the MDAR performance and characteristics should disregard this section and proceed directly to Section 2 "Maintenance Tests".

1.1 NON-PILOT PERFORMANCE TESTS

To prepare the MDAR relay assembly for Non-Pilot Acceptance Tests, connect the MDAR per **Figure H-1**, Configuration 1.

1.1.1 Front Panel Check

Step 1.Turn on rated battery voltage. Check the FREQ setting to match the line frequency and ct type CTYP. Apply a balanced 3-phase voltage (70 Vac); the Alarm-1 relay should be energized. (Terminals TB4-7 and -8 should be zero ohms.)

Step 2. Check "RELAY-IN-SERVICE" LED; it should be "ON".

Step 3. Press "RESET TARGETS" push-button; the green LED (Volts/Amps/Angle) should be "ON".

Step 4. Using a dc voltmeter, measure the dc voltages on the front panel display with respect to common (± 5%).

Step 5. Press the DISPLAY SELECT pushbutton, and note that the mode LED cycles thru the five display modes. Release the pushbutton so that the SETTINGS mode LED is "ON".

Step 6. Refer to the Installation Section, **Table 4-1**, for all possible MDAR SETTINGS, and set the values in accordance with **Table H-1**. For Negative Sequence Directional Unit, change DIRU from ZSEQ to NSEQ. For dual polarizing directional ground unit, change DIRU to DUAL.

Step 7. Press the DISPLAY SELECT pushbutton to obtain the METERING mode (VOLTS/ AMPS/ ANGLE). (Refer to Installation Section, Table 4-2.)

1.1.2 Angle Current and Voltage Input Check

Step 8. Using **Figure H-1**, Configuration 1, apply three ac voltages of 70 V_{LN} and an ac current of 1A. Adjust phase A current to lag phase A voltage (V_{AN}) by 75°.

Step 9. Press FUNCTION RAISE or FUNCTION LOWER pushbutton. Read input current (IA), input voltage (V_{AG}), and angle (ANG). All values within 5%.

NOTE: Be sure that the RP setting is "NO". If the RP setting is "YES", the readings will be the primary side values.

The angle measurement is for reference only. For I<0.5A, the display of angle will be blocked and show zero degrees.

1.1.3 Zone-1 Test/Single-Phase-To-Ground

Step 10. Using **Figure H-1**, Configuration 1, adjust:

V_{1N} = 30V

V_{2N} = 70V

V_{3N} = 70V

MDAR goes into fault mode processing only after the current detector is enabled. MDAR performs the test:

- Phase current (ΔI_A, ΔI_B, or ΔI_C) >1.0A peak and 12.5% change
- Ground current (ΔI_0)>0.5 A peak
- Voltage (ΔVan, ΔVbn, or ΔVcn) >7V and 12.5% change with a current change of ΔI>0.5 A

When one of the above is true, MDAR starts fault processing. In order to perform the above, apply a certain value of current *suddenly.* If MDAR does not trip, turn the current off, readjust to a higher value, and then *suddenly* reapply current.

The current required to trip can be calculated using the following:

$$I = \frac{V_{LN}}{Z_{1G}\,COS(PANG - X)\left[1 + \frac{(Z_R - 1)}{3}\right]}$$

From Table H-1:

- Z1G = 4.5 Ω
- PANG = 75°
- ZR = 3.0

using an X = 75° (lagging)

The current required to trip = 4.00A ± 5 % for fault current lagging fault voltage by 75°. This is the maximum torque angle test. For other points on the MHO circle, change X to a value between 0° and 150°, and calculate the value of I.

See **Table 4-3**, for a description of the following displayed fault data for:

- Fault Type (FTYP)
- Targets (BK1, Z1G)
- Fault Voltages (V_A, V_B, V_C, $3V_0$) and Currents (I_A, I_B, I_C, $3I_0$)

With the external jumper connected between TB1-13 and TB1-14, the BFIA-1, BFIA-2 should be closed. The GS contact will be ON for approximately 50 ms. when the fault is applied. Alarm-2 relay will be picked-up, which can be reset by the RESET button after the fault is removed. Change TTYP to 1PR; the RI2-1 and RI2-2 should be CLOSED. Change TTYP to 2PR (or 3PR). Repeat test; RI2-1 and RI2-2 should be closed. Change TTYP to "OFF". Repeat test. RI2-1, RI2-2 should not be picked-up.

Repeat AG fault and measure the trip time, which should be < 2 cycles. Change the setting of T1 from No to Yes. Repeat the test; the trip time should extend for an additional 2 cycles. Reset T1 to zero.

The following formula can be used when PANG ≠ GANG:

$$Vxg = (I_X + K_0\, I_0)\, Zcg$$

or $$Vxg = \left(I_x + \frac{K_0 I_x}{3}\right) Zcg$$

or $$I_X = \frac{V_{xg}}{Z_{cg}\left(1 + \frac{K_0}{3}\right)}$$

where

$$K_0 = \frac{(Z_{0L} - Z_{1L})}{Z_{1L}}$$

$$= |Z_R| \angle (GANG - PANG)\ -1$$

$$I_X = \frac{V_{xg}}{|Z_{cg}| e^{jPANG}\left[1 + \frac{|Zr| e^{j(GANG - PANG) - 1}}{3}\right]}$$

or $$I_X = \frac{V_{xg}}{\frac{2}{3}|Z_{cg}| e^{jPANG} + \frac{1}{3}|Z_{cg}||Zr\ | e^{jGANG}}$$

Example:

Vag = 30 Z1g = 4.5 PANG = 85
GANG = 40 Zr = 3

$$Ia = \frac{30}{\frac{2}{3}(4.5)e^{j85} + \frac{1}{3}(4.5)(3)e^{j40}}$$

$$= \frac{30}{3\cos(85) + j\,3\sin(85) + 4.5\cos(40) + j4.5\sin(40)}$$

$$= 4.31\angle(-57.76)$$

This is the trip current (4.3A) at the maximum torque angle of -57.76° (current lags voltage by 57.76°).

The following equation should be used for the angle of x on the MHO circle:

$$Iax = \frac{30}{6.96\cos(57.76 - x)}$$

Step 11. Using **Figure H-1**, Configurations 2 and 3, repeat (preceding) Step 10 for BG and CG faults. Note Targets**.**

1.1.4 Zone-1 Test/Three-Phase

Step 12. Using **Figure H-2**, connect current and voltage circuits and apply:

- V_{AN} = 30V ∠0° IA = 6.67 ∠–75°
- V_{BN} = 30V ∠–120° IB = 6.67 ∠–195°
- V_{CN} = 30V ∠120° IC = 6.67 ∠+45°

Using a value of x = 75° (lagging), the current required to trip is calculated as follows (Note Targets):

$$I = \frac{V_{LN}}{Z_{1P}\cos(PANG - X)} = 6.67A \pm 5\%$$

Since V2.6x uses $I_A + I_B + I_C$ to calculate $3I_0$, a balanced 3-phase current source is recommended to be used for this test ($3I_0$ = 0). **Figure H-2** gives a concept of the test. If a Doble or Multi-Amp test set is used, be sure to synchronize the 3-phase currents. If possible, use a multi-trace storage scope to verify the waveforms of I_A, I_B and I_C.

In order to plot the MHO circle for different input angle (X), the setting of RT (and RU, if OSB option is included) should be at maximum (15 ohms). Refer to OSB test for detailed information. Set TTYP = 3PR. Repeat test; RI2-1 and RI2-2 should be closed. For TTYP = OFF, or 1PR, or 2PR repeat the test. RI2-1 and RI2-2 should be open.

1.1.5 Zone-1 Test/Phase-To-Phase

Step 13. Two methods can be used for this test.

a. Using T-connection (with Doble or Multi-Amp Test Unit; refer to **Figure H-3** for external terminal connection and configuration 1.

- V_A = 1/2 V_F @ 0°
- V_B = 1/2 V_F @ 180°
- V_C = 3/2 (70) = 105V @ 90° lead

Using $V_F = V_A - V_B$ = 30V

The following table is for BC and CA fault tests when the T-connection is used:

BC		CA	
V_{AN}	= 105 ∠90°	V_{AN}	= 15 ∠180°
V_{BN}	= 15 ∠0°	V_{BN}	= 105 ∠90°
V_{CN}	= 15 ∠180°	V_{CN}	= 15 ∠0°
I_F	= 3.33 ∠-75°	I_F	= 3.33 ∠–75°

- V_A = 15V @ 0°
- V_B = 15V @ 180°

NOTE: Current (I_A) required to trip = 3.33A ±5%, with an angle of -75 degrees.

b. Using Y-connection

NOTE: This test is actually for ϕϕG testing (see Figure H-3, configuration 1).

$$V_{AN} = \frac{1}{2} V_F \left(\frac{2}{\sqrt{3}} \angle 0°\right)$$

$$V_{BN} = \frac{1}{2} V_F \left(\frac{2}{\sqrt{3}} \angle -120°\right)$$

$$V_{CN} = \left(\frac{3}{2} \times 70 - \sqrt{|V_{AN}|^2 - \left|\frac{1}{2}V_F\right|^2}\right) \angle 120°$$

or

$$V_{AN} = 17.3 \angle 0°$$

$$V_{BN} = 17.3 \angle -120°$$

$$V_{CN} = 96.4 \angle 120°$$

For either T or Y connection, using a value of x = 75° (lagging), current required to trip:

$$I = \frac{V_F}{2Z_{1P}\cos(PANG - X)}$$

From Table H-1:

- Z_{1P} = 4.5 Ω
- PANG = 75°

For Y-connection only, current (IA) required to trip = 3.33A ±5%, with an angle of -45°, because Ian has already lagged V_F (V_{ab}) by 30°. Review all targets.

NOTE: The accuracy of the voltage reading in the metering mode is between 1 and 77 Vrms. The inaccurate reading on V_{CN} will not affect the results of the test.

The reclose contacts (RI2-1 and RI2-2) should be closed for setting of TTYP = 2PR or 3PR, and should be open for TTYP = OFF or 1PR.

Step 14. Repeat Step 13 for both BC and CA faults. Use the following voltages for each fault type:

BC	CA
$V_{AN} = 96.4\angle 120°$ V	$V_{AN} = 17.3\angle -120°$ V
$V_{BN} = 17.3\angle 0°$ V	$V_{BN} = 96.4\angle 120°$ V
$V_{CN} = 17.3\angle -120°$ V	$V_{CN} = 17.3\angle 0°$ V
$I_F = 3.33\angle -45°$	$I_F = 3.33\angle -45°$

1.1.6 Zone-2 Tests

Step 15. Press the DISPLAY SELECT pushbutton until the SETTINGS mode LED is displayed. Change the setting values to:

- Z1P = “OUT” (Zone-1 phase value)
- Z1G = “OUT” (Zone-1 ground distance)
- Z2P = 4.5 Ω (Zone-2 phase value)
- T2P = 1.0 sec (Zone-2 phase timer)
- Z2G = 4.5 Ω (Zone-2 ground value)
- T2G = 1.5 sec (Zone-2 ground timer)
- Z2RI = “YES” (Zone-2 reclosing)
- TTYP = “3PR” (Reclosing mode)

Step 16. Perform Steps 10 thru 14 (above) for Zone-2 only, using delayed trip times according to the Zone-2 phase timer (T2P), and the Zone-2 ground timer (T2G). Tolerances for T2P and T2G are 5% for an input current that is 10% above the calculated value.

Repeat Step 10. The RI2 contacts 1 and 2 should be closed, and the RB contacts 1 and 2 should be open. Reset Z2RI to “NO”.

Repeat Step 10 again. The RI2 contacts 1 and 2 should be open and the RB contacts 1 and 2 should be closed.

Change the settings of T2G and T2P to BLK. Zone-2 should not be tripped for any type of fault.

1.1.7 Zone-3 Tests

Step 17. Press the DISPLAY SELECT pushbutton until the SETTINGS mode LED is displayed. Change the setting values to:

- Z2P = “OUT” (Zone-2 phase value)
- Z2G = “OUT” (Zone-2 ground distance)
- Z3P = 4.5 Ω (Zone-3 phase value)
- T3P = 2.0 sec (Zone-3 phase timer)
- Z3G = 4.5 Ω (Zone-3 ground value)
- T3G = 2.5 sec (Zone-3 ground timer)
- Z3FR = “FWD” (Zone-3 direction)
- Z3RI = “YES” (RI = Z3T)
- TTYP = “3PR” (Reclosing Mode)

Step 18. Perform preceding steps 10 thru 14 for Zone-3 only, using delayed trip times according to the Zone-3 phase timer (T3P), and the Zone-3 ground timer (T3G). Tolerances for T3P and T3G are ±5% for an input current that is 10% above the calculated value.

Repeat Step 10. The RI2 contacts 1 and 2 should be closed, and the RB contacts 1 and 2 should be open. Reset Z3RI to “NO”.

Repeat Step 10 again. The RI2 contacts 1 and 2 should be open and the RB contacts 1 and 2 should be closed.

Step 19. Set Z3FR = REV, then repeat Step 10, except apply AG reversed fault (i.e., I_a leads Van by 105°). The relay should trip, at I_a = 4.2A, in 2.5 seconds. Reset Z3FR to “FWD”.

NOTE: For customers who use a computer to test the relays, or use their own settings for maintenance, refer to the following

example to calculate and determine trip currents; set the relay as follows:

Z1P = ZIG = 4.5 T1 = 0

Z2P = Z2G = 6.0 T2P = T2G = 0.2

Z3P = Z3G = 9.0 T3P = T3G = 0.3

PANG = GANG = 75° ZR = 3

a. Single-Phase-to-Ground Fault

Use the equation in Step 10, and the following input voltages:

$V_{AN} = 45\angle 0° = V_{LN}$

$V_{BN} = 70\angle -120°$

$V_{CN} = 70\angle 120°$

The single-phase trip currents for Zone-1, Zone-2, and Zone-3 at the maximum torque angle $(I_A\angle 75°)$ are 6.0A, 4.5A and 3.0A, respectively.

b. Phase-to-Phase Fault

Use the T-connection and the equation in step 13. Apply the following input voltages:

$V_{AN} = 18\angle 0° = \frac{1}{2}V_F$

$V_{BN} = 18\angle -180° = \frac{1}{2}V_F$

$V_{CN} = 105\angle 90°$

The single-phase trip currents for Zone-1, Zone-2 and Zone-3 at the maximum torque angle $(I_{AB}\angle -75°)$ are 4A, 3A and 2A, respectively.

c. Three-Phase Fault

Use the equation in Step 12 with the following input voltages:

$V_{AN} = 27\angle 0° = V_{LN}$

$V_{BN} = 27\angle -120°$

$V_{CN} = 27\angle 120°$

The three-phase trip currents for Zone-1, Zone-2 and Zone-3 at the maximum torque angles

$(I_A\angle -75°, I_B\angle -195°, I_C\angle +45°)$

should be 6.0A, 4.5A and 3.0A, respectively.

1.1.8 Instantaneous Overcurrent (High-Set Trip)

Step 20. Using the SETTINGS mode, change the following settings:

ITP = 10A	LOPB = "NO"
ITG = 5A	Z3G = "OUT"
	Z3P = "OUT"

NOTE: The High-Set ground overcurrent (ITG) and phase overcurrent (ITP) are supervised by Forward Directional Ground unit (FDOG) and Forward Directional Phase unit (FDOP), respectively. In order to test the High-Set trip, the 3ϕ voltages are necessary as directional reference. The ITG and ITP will automatically become non-directional overcurrent units if the setting of LOPB is YES and at least one input voltage is zero volts (e.g., LOPB = YES in the metering mode).

Step 21. Using **Figure H-1**, configuration #1, to connect currents and voltages, apply AG fault as shown in Step 1.1.3. The MDAR should trip at I_a = 5 Amps ± 5 % with a target of ITG-AG. For reversed fault, apply 10A reversed fault current (i.e., I_a leads Van by 135° for Y-connection, or 105° for T-connection). The relay should not trip.

Step 22. Using **Figure H-3**, to connect currents and voltages, apply AB fault as shown in Step 1.1.5. The MDAR should trip at Iab = 10 Amps ±5%, with a target of ITP - AB. Apply a 15A reversed fault current (i.e., I_a leads V_{ab} by 135° for Y-connection or 105° for T-connection). The relay should not trip.

1.1.9 Ground Backup (GB) Test

Step 23. Use the SETTINGS mode and change the following settings:

- ITP = "OUT"
- ITG = "OUT"
- GBCV = CO-8
- GBPU = .5
- GDIR = "NO"

• GTC = 24

NOTE: The note in Step 20 applies to the GB test. The GB can be set to directional ground overcurrent. For loss-of-potential condition, GB will be converted to non-directional, automatically, regardless of the GDIR=YES setting.

Using **Figure H-1**, apply A-G fault of 4.1A to MDAR. Trip time is determined as follows:

$$(T_{MSEC}) = \left[478 + \frac{4122}{3I_0 - 1.27}\right]\frac{GTC}{24}$$

where $3I_0 = \frac{3I_{OF}}{GBPU}$

($3I_{OF}$ is zero sequence fault current.)

$$(T_{MSEC}) = \left[478 + \frac{4122}{4.1/0.5 - 1.27}\right]\frac{24}{24}$$

T_{MSEC} = 1073 msec

= 1.073 sec ±5% to trip

For values of $3I_0$ between 1.0 and 1.5, the following equation would apply:

$$(T_{MSEC}) = \frac{(9200)}{3I_0 - 1} \times \frac{GTC}{24} (CO-8 \text{ only})$$

The following equation can be used to calculate the trip time for all CO curves from CO-2 to CO-11:

T(sec) =

$$\left[T_0 + \frac{K}{(3I_0 - C)^p}\right] \times \frac{GTC}{24,000} \quad (\text{for } 3I_0 \geq 1.5)$$

$$T(sec) = \frac{R}{(3I_0 - 1)} \times \frac{GTC}{24,000} \quad (\text{for } 1 < 3I_0 < 1.5)$$

where $3I_0 = \frac{3I_{OF}}{GBPU}$

GBPU = Pickup current setting (0.5 to 4.0A).

GTC = Time curve dial setting (1 to 63).

T_o, K, C, P and R are constants, and are shown in Table H-2.

Step 24. For a Zero Sequence Directional unit (DIRU = ZSEQ), the tripping direction of MDAR is: the angle of $3I_0$ leads $3V_0$ between +30° and +210°. Change the setting of GDIR to "YES". Apply AG fault as shown in preceding Step 10, **Figure H-1**. The relay should trip at the following angles:

• +28°
• -60° (± 88°)
• -148°

The relay should *not* trip at the angles of:

• +32°
• +120° (± 88°)
• -152°

For a Negative Sequence Directional Unit (DIRU = NSEQ), the tripping direction of MDAR is: I_2 leads V_2 by a value between +8° and +188°. The relay should trip at the following angles:

• +3°
• -82° (± 85°)
• -167°

The relay should not trip at the angles of:

• +13°
• +98° (± 85°)
• +183°

Step 25. For a dual polarizing ground directional unit (DIRU = DUAL) test, connect the test circuit shown in **FigureH-4;** apply Lp $1.0A\angle -90°$ to terminals 12 (+) and 11(-), and apply a balanced 3-phase voltage (70V) to Va, Vb, Vc, and Vn. Apply Ia = 4A to terminals 6(+) and 5(-).

NOTE: In order to eliminate the voltage polarizing effect, make sure the voltages are finely balanced so that 3V0 is less than 1.0 volt.

The relay should trip at the following angles:

• -3°
• -90° (± 87°)
• -177°

The relay should <u>not</u> trip at the following angles:

• +3°
• +90° (±87°)
• +177°

1.1.10 CIF, STUB, IOM, IL and LV Tests

Step 26. Set the relay per **Table H-1**. Change the following settings: IOM = 3, IL = 2, CIF = CIFT, and connect a rated dc voltage to 52b, between TB5/3 (+) and TB5/4 (-). Apply an AG fault as shown in Step 10 (**Figure H-1**). The relay should trip at I_a = 2A (IL) with CIF target. Change IL setting from 2 to 3.5A and repeat the test shown in Step 26. The relay should trip at I_a = 3A (IOM) with CIF target.

Step 27. LV setting test. Set LV = 60 and with I_{AN} = 4A, apply AG fault as shown in Step 10. The CIF trip should be for V_{AN} <60 Vrms ± 5%.

Step 28. For STUB Bus Protection (SBP), check the blue jumpers on the Interconnect module. JMP7 and 9 should be IN; JMP13 should be at the rated voltage position. Select CIF = STUB. Disconnect the voltage from 52b and connect it to terminals TB5/13(+) and TB5/14(-).

NOTE: Make sure the jumpers (JMP8 and JMP10) are not IN before applying the voltage to TB5/13(+) and TB5/14(-).

Apply I_A = 4A. The STUB bus trips for any V_{AN} voltage with a target of CIF. Disconnect the voltage from SBP and reset IOM = I_L = 0.5 and CIF = NO.

1.1.11 Loss-of-Potential (LOP) Test

Step 29. For Load Loss Trip (LLT), set:

LLT = Yes

Z2P = Z2G = 4.5 ohms

T2P = T2G = 2.99 sec (or BLK)

Apply:

Va = $30\angle 0°$

Vb = $70\angle -120°$

Vc = $70\angle 120°$

Ia = $3.5\angle -75°$

Ib = $1\angle -120°$

Ic = $1\angle +120°$

Suddenly increase Ia from 3.5 to 4.5A and then turn I_b OFF immediately. The relay should trip with LLT target. The trip is accelerated due to the pickup of Zone-2 and the setting of LLT = YES.

Change the setting of LLT = FDOG and the input current I_a from 1.5 to 2.5A; then turn I_b OFF immediately. The relay should trip with a target of LLT. The trip is due to the pickup of FDOG and setting of LLT = FDOG.

Reset: LLT = NO

Z2P = Z2G = OUT

T2P = T2G = BLK

Step 30. Disconnect all current inputs. Connect 3 balanced voltages of 70 Vac to V_{an}, V_{bn}, and V_{cn}. Using the SETTINGS mode, change the setting: LOPB = YES.

NOTE: The "RELAY IN SERVICE" LED will not be turned "OFF" for the condition of setting LOPB = Yes, but Zone-1, 2, 3 and pilot distance units will be blocked and all overcurrent units (GB, ITP, and ITG) will be converted to non-directional operation.

LOPB will be set if the following logic is satisfied:

- one (or more) input voltages (V_{AN}, V_{BN} or V_{CN}) are detected (as <7 Vrms) without ΔI change, **or**
- a 3Vo (> 7Vrms) is detected with 3Io <Ios
- Apply V_{AN}, V_{BN} and V_{CN} rated voltage to MDAR. Scroll the LED to metering mode; the display shows LOPB = NO. Reduce VAN to 62 Vrms (e.g., $3V_0$ = 8V). After approximately 0.5 seconds, the display shows LOPB = YES and the form C failure alarm (AL1) contact is also deenergized.

Step 31. Set the relay as follows:

Z1P	= 4.5	GBCV	= CO-8
Z1G	= 4.5	GBPU	= 0.5
ITP	= 10	GDIR	= YES
ITG	= 5	GTC	= 24

Repeat Step 10 (AG Fault) with I_{AN} = 4.5A. While in the metering mode, be sure that LOPB = YES before the fault current is applied. The relay should be tripped with a target of GB. Apply 5.5A; the relay should be tripped with a target of ITG.

Repeat the test with a reversed AG Fault; the relay will trip. Reset LOPB = NO; the relay should not trip for the reversed fault. Set LOPB = YES.

Step 32. Apply a balanced three-phase voltage (70 Vrms) and current (3A). Turn off Va; the relay should not trip. Reset LOPB to NO.

1.1.12 Loss-Of-Current (LOI) Test

Step 33. Set LOIB to YES and I_{OM} = 1.0A. Apply a balanced three-phase voltage (70 Vrms). Connect the current inputs per **Figure H-1**, and apply a single phase current of 1.1A to I_A. After approximately 0.5 seconds, the "Relay In Service" LED will be turned off, and the Form C failure alarm (AL1) contact will be dropped out (deenergized) indicating a failure condition.

Step 34. Increase I_A to 1.5A. Depress the DISPLAY SELECT pushbutton and change to the metering (VOLTS/AMPS/ANGLE) mode. Press FUNCTION RAISE pushbutton until the LOI display is shown. The value should indicate "YES". Suddenly turn OFF V_A voltage; the relay should not be tripped within 500 ms. It may operate after 500 ms if a delta I is detected by the relay. Change the setting of LOIB from YES to NO.

1.1.13 Output Contact Test

Step 35. The purpose of this test is to check the hardware connections and relay contacts. It is designed for a bench test only. Remove JMP12 (spare on the Microprocessor PC Board) and place it in the JMP5 position. Open the red-handled FT switch (Trip and Breaker Failure Initiate) in order to avoid the undesired trip.

NOTE: The red-handled FT switch (#13) controls the dc supply of BFI, RI2 and the optional RI1 relays. In order to test these relays in the system, the external wiring should be disconnected to avoid undesired reclosing or trip. For relays without FT switches, *do not* perform the Output Contact tests using the relay system.

Change the LED mode to "TEST" and select the tripping function field and the desired contact in the value field. Push the ENTER button; the ENTER LED should be "ON". The corresponding relay should operate when the ENTER button is pressed. The following contacts can be tested:

- TRIP
- BFI
- RI1 (optional)
- RI2
- RB
- AL1 (with three balanced voltages applied)
- AL2
- GS
- SEND
- STOP
- OC 1 TO OC8 (optional)

Remove JMP5 and replace it on JMP12.

Step 36. This completes the basic Acceptance Test for the MDAR Non-Pilot system. (See subsequent segment for optional Single Pole Trip and Out-of-Step Block tests.)

1.2 PILOT PERFORMANCE TESTS

To prepare the MDAR relay assembly for Pilot Acceptance Tests, connect the MDAR per **Figure H-1**, Configuration 1.

NOTE: For Power Supply module sub 13 or higher, three Reed relays are used to replace the mercury relays for GS, Carrier STOP and SEND. Check jumpers JMP1 (STOP) and JMP2 (SEND) for NO or NC output contact selection.

1.2.1 Front Panel Check

Step 1. Repeat steps 1 thru 6 in Non-Pilot Acceptance Tests.

Step 2. Change the value settings, in Table H-1, as follows:

• PLT	YES	• PLTP	6.0
• Z3FR	REV	• Z3P	6.0
• ZIP	OUT	• Z3G	6.0
• ZIG	OUT	• T3P	BLK
• PLTG	6.0	• T3G	BLK

NOTE: When the dc voltage is applied to TB5 terminals, check jumper position on Interconnect module for the appropriate selection.

Connect a rated dc voltage to PLT/ENA terminals TB5/9(+) and TB5/10(-).

1.2.2 Blocking (BLK) Scheme

Step 3. Change the STYP setting to BLK. Apply a rated dc voltage to RCVR #1 terminals TB5/7(+) and TB5/8(-). Check the metering mode for RX1 = YES. Apply an AG fault as shown in Step 10 of the Non-Pilot Acceptance Test (i.e., V_a = 30 volts and I_a = 4 Amps). The trip A contacts should not be closed. The CARRY SEND should be "open" and the CARRY STOP should be "closed".

Step 4. Remove the dc voltage from RCVR #1 and apply AG fault. Trip A contacts should be "closed" and the target should show "PLTG AG".

Change the LED mode to "TEST" and select the "RS1" function. Push the ENTER button; the ENTER LED should be "ON". Repeat Step 4 with the ENTER button depressed. The relay should not trip.

Step 5. Apply AG reversed fault (i.e., I_a leads V_a by 105 degrees). The CARRY SEND contacts should be "closed" and the CARRY STOP contacts should be "open". (I_a should be > 3A for the Zone-3 setting of 6 ohms.)

Step 6. Change the LED mode to TEST and select the function "TK". Push the ENTER button; the ENTER LED should be "ON" and the CARRY SEND contacts should be closed.

Step 7. In order to determine setting accuracy (6 ohms), the forward directional ground unit must be disabled. Set FDGT = BLK. Repeat preceding Step 4 of the Pilot Acceptance Test, with a trip input current (I_a) of 3 Amps (± 5%).

Step 8. Set the Forward Directional Ground Timer (FDGT) from 0 to 15 cycles. Repeat Step 4 with I_a = 1.5 A. The relay should be tripped after the delay time of FDGT.

NOTE: The FDOG trip is determined by the IOM **setting. It trips if $3I_0$ >**IOM **and the forward ground directional unit picks up.**

Step 9. In order to perform the Breaker Failure Reclose Block Test, change the setting of FDGT = 0 and BFRB = NO. Repeat test Step 4; RB contacts (TB3/1 and TB3/2) should not close. Change BFRB to YES and repeat the test. The RB contacts should be closed with a time delay between 150 ms and 200 ms.

NOTE: For Va = Vb = Vc = 0, Ia = Ib = Ic = 0, the setting of OSB = YES, WFEN = NO, and the input of 52b = OV, the carrier SEND contacts will be closed. This is not desirable, but occurs only on the test bench. If tested with the relay system, V = 0 and I = 0 mean that the 52b input is at a rated voltage which will stop the SEND signal.

1.2.3 PUTT or POTT Schemes

Step 10. Change the setting to STYP = PUTT (for underreach scheme) or STYP = POTT (for overreach scheme). In order to determine setting accuracy (6 ohms), the forward directional ground unit must be disabled. Set FDGT = BLK. Apply a rated voltage to RCVR #1 terminals TB5/7(+) and TB5/8(-), and apply an AG fault as shown in Step 10 of the Non-Pilot Acceptance Test. The trip contact A should be closed at the input I_a = 3A (± 5%); the target should show "PLTG AG", and the CARRY SEND contact should be "closed" for POTT setting. Do not test carry STOP for POTT and PUTT schemes.

Step 11. Apply a reversed AG fault (I_a leads V_a by 105°). The relay should not trip, and the CARRY SEND contact should stay "open".

Step 12. Remove the voltage on RCVR #1. Apply a forward AG fault as shown in Step 10. The trip contacts should remain "open" for I_a = 5A.

Step 13. Change the LED mode to TEST and select the function "RS1". Push the ENTER button; the ENTER LED should be "ON". Repeat Step 12 with the ENTER button depressed. The relay should trip.

Step 14. Repeat steps 8 and 9 for FDGT and BFRB tests, by using Step 10 with Ia = 1.5 A.

1.2.4 Weakfeed Scheme

Step 15. This function is for POTT only. In addition to the setting changes in Step 2, change the following settings:

- STYP POTT
- WFEN YES
- Z3G 4.5
- Z3P 4.5
- Z3FR REV

Apply a rated voltage to PLT/ENA terminals TB5/9(+) and TB5/10(-), also RCVR #1 terminals TB5/7(+) and TB5/8(-).

With $V_{an} = V_{bn} = V_{cn}$ = 70 Vrms applied (as shown in **Figure H-1**), the relay should operate normally.

NOTE: Do not apply fault current.

Turn V_{an} "OFF"; the relay should trip with a target of WFT, and the Carrier Send contact (TB4-1 and TB4-2) should close momentarily.

Reduce Van from 70 Vrms to 69Vrms and apply a reverse AG fault current of 5A (i.e., I_a leads V_{an} by 105 degrees). Turn V_{an} "OFF"; the relay should not trip, and the Carrier Send contact (TB4-1 and TB4-2) should stay open.

Step 16. This completes the basic Acceptance Test for the MDAR Pilot System. (See subsequent segments for optional Single Pole Trip test.)

1.3 SINGLE POLE TRIP (OPTION) ACCEPTANCE TESTS

Step 1. Set relay per **Table H-1**. Check the 62T setting; it should be 5.000. For a Pilot System, change the setting to PLT = YES, and apply a rated dc voltage to Pilot Enable terminals TB5/9(+) and TB5/10(-). Also apply a rated voltage to RCVR #1 terminals TB5/7(+) and TB5/8(-) if the STYP = POTT or PUTT; set TTYP = SPR.

Apply AG fault as shown in this Appendix Section 1.1.3, Step 10. The Trip A contacts (2FT-14/1-2 and 3-4) should be closed. Repeat BG fault (for Trip B contact closures) and repeat CG-Fault (for Trip C contact closures).

1.3.1 Sound Phase Fault (SPF) and 62T Trip

Step 2. Apply a rated dc voltage to 52a terminals TB5/1(+) and TB5/2(-) and to 52b terminals TB5/3(+) and TB5/4(-). Connect a Lockout to the trip circuit.

Step 3. Apply a phase-to-phase fault (as shown in this Appendix, segment 1.1.5, Step 13). Turn the fault current "ON" and "OFF". The lockout relay trips with a target of SPF.

Step 4. Reset the lockout relay immediately; it will trip again with a target of 62T. Remove the voltages from 52a and 52b.

1.3.2 Reclose (RI) Trip and Breaker Failure (BFI) Contacts

Step 5. Refer to the Non-Pilot Acceptance Test for the single-phase-to-ground faults (Steps 10 and 11), and to the three-phase fault (Step 12). The fault current should be 20% greater than the calculated values for the tests in these steps. The "fault types" applied to the MDAR relay are shown in **Table H-3** (column 2). TTYP settings are shown in column 1, whereas the results of RI, Trip, and BFI contacts are shown in columns 3, 4, and 5, respectively.

1.4 MDAR WITH OUT-OF-STEP BLOCK OPTION

Refer to **Figure H-5**. The RT setting (21BI) is for the inner blinder and it is also used for three-phase fault load restriction. The RU setting (21BO) is for the outer blinder. If the setting of OSB is "YES", and the power swing stays inside the two parallel lines (RT and RU) for more than 50 ms, the three-phase fault trip will be blocked until the timer (OSOT) times out.

Connect the test circuit as shown in **Figure H-2**.

1.4.1 Condition OSB = NO

Step 1. Set the relay per **Table H-1**, except for the following settings:

Z1P = 10

Z1G = 10 T2P = 0.1

Z2P = 20 T2G = 0.1

Z2G = 20

(Check: PANG = GANG = 75; RT = RU = 15; OSOT = 4000)

Step 2. Adjust the inputs as follows:

$V_a = 40\angle 0°$ $I_a = I_F\angle -45°$

$V_b = 40\angle -120°$ $I_b = I_F\angle -165°$

$V_c = 40\angle 120°$ $I_c = I_F\angle 75°$

Step 3. Apply current I_F of 2.35A ±5% suddenly. The relay should trip with a display of Z2P = ABC.

Step 4. Apply I_F of 4.7A ± 5% suddenly. The relay should trip with a display of Z1P = ABC.

Step 5. Change the RT setting from 15 to 4. Repeat Steps 3 and 4 (above). The relay should not trip because the RT restricts the 3-phase fault current.

NOTE: The trip current (I_F) can be obtained from the equation in test Step 12 (1.1.4 Zone-1 Test/Three-Phase), with the parameters:

VLN = 40 PANG = 75

Z1P = 10 (or Z2P = 20) X = 45

1.4.2 Condition OSB = YES

Change the OSB setting from NO to YES and RT = 4, RU = 8.

Step 1. Change the LED to metering mode with the display of OSB = NO.

Step 2. Apply a current I_F of 2.7A ± 5% suddenly. The display should show OSB = YES for 4 seconds. This means the input power swing is inside the outer blinder (2IBO). Repeat this test for I_F = 4A and 4.5A. The display should show OSB = YES because the power swing is within two blinders (2IBO and 2IBI).

Step 3. Apply a current of 4.5A and increase the I_F to 5.5A immediately. The relay should trip with a display of Z2P = ABC (or Z1P = ABC). This means the power swing stays inside the blinders for more than 50 ms and then crosses over 21BI. For the current of 4.5A, Z1P or Z2P may pick up, but the relay trips after the OSOT timer times out.

Step 4. Apply I_F of 5.25A suddenly (5% above the calculated value). The relay should trip with a display Z1P = ABC. The trip time should be <2 cycles.

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Appendix H-2. ACCEPTANCE/MAINTENANCE TESTS (V2.10)

2. MAINTENANCE QUALIFICATION TESTS

Maintenance qualification tests will determine if a particular MDAR unit is working correctly. ***Refer to the WARNING note in Section H-1 before energizing the relay.***

2.1 NON-PILOT MAINTENANCE TESTS

It is recommended that either Doble or Multi-Amp test equipment should be used for this test. Refer to **Figure H-1** for the input voltage and current terminal connection per configuration 1. Check all jumper positions on the Interconnect module for rated dc voltage.

2.1.1 Front Panel and Metering Check

Step 1. Turn on rated dc voltage. Check the FREQ setting; it should match the line frequency and ct type (CTYP). Apply a balanced 3-phase voltage (70 Vac); the Alarm-1 relay should be energized. (Terminal TB4/7 and TB4/8 should be zero ohms.) The "Relay-in-Service" LED should be "ON".

Step 2. Press RESET pushbutton; the green LED (Volts/Amps/Angle) should be "ON". Press the FUNCTION RAISE or FUNCTION LOWER pushbutton. Read the input voltages and their angles:

VAG = 70 ∠0°
VBG = 70 ∠–120°
VCG = 70 ∠120°
with an error of ± 1 volt and ± 2°.

Step 3. Press the DISPLAY SELECT pushbutton, and note that the mode LED cycles thru the five display modes. Release the pushbutton so that the SETTINGS mode LED is "ON". Press the RAISE button to scroll thru the FUNCTION FIELD to check the settings per Table H-1. Change the setting, if necessary, by depressing the RAISE button in the VALUE FIELD to the desired value and then pressing the ENTER button.

Step 4. Press the RESET pushbutton (LED jumps to Metering mode). Apply 3.0 A to I_A with an angle of -75°. Read I_A from the front display; it should be 3.0 ∠–75° with an error of 5% and ± 2°. Move the input current from IA to IB or IC terminal. Read I_B or I_C to verify the transformer's accuracy.

2.1.2 Impedance Accuracy Check

Step 5. Apply voltages to MDAR as follows:

V_A = 30 ∠0°
V_B = 70 ∠-120°
V_C = 70 ∠120°

Apply forward fault current I_A ∠-75° suddenly. The relay should trip for I_A = 4A ± 5%. The display should show "Z1G AG".

Repeat for B and C phases per the following table:

Phase B	**Phase C**
V_A = 70 ∠120°	V_A = 70 ∠-120°
V_B = 30 ∠0°	V_B = 70 ∠120°
V_C = 70 ∠-120°	V_C = 30 ∠0°
I_B = 4 ∠-75°	I_C = 4 ∠-75°

2.1.3 Input Opto-Coupler Check

Step 6. External Reset
Apply an AG fault as shown in Step 5. The LAST FAULT LED should be flashing. Press the front RESET pushbutton. The green LED (Volts/Amps/Angle) should be "ON". Press the DISPLAY SELECT pushbutton and move the LED back to LAST FAULT. The fault information "Z1G AG" should be displayed again. Apply a rated dc voltage to terminals TB5/5 (+) and TB5/6(-). The target data should be erased and the display should show "FTYP". Remove the external reset voltage.

Step 7. 52b Terminals
Change the CIF setting from "NO" to "CIFT". Apply an AG fault as shown in Step 5, with I_A = 2 ∠–75°. The relay should not trip. Apply a rated dc voltage to terminals TB5/3 (+) and TB5/4 (-). Repeat the test. The relay should trip with a target of CIF. Remove the 52b voltage and set CIF to STUB for the next test.

Step 8. Stub Bus Protection (SBP)

Check the blue jumpers on the Interconnect module. Jumpers (JMP 7 and JMP 9) should be "IN". JMP 13 should be at the rated voltage position. Apply a balanced 3-phase voltage (70 Vac and I_A = 2A) using any angle. The relay should not trip. Apply a rated voltage to the SBP terminals: TB5/13(+) and TB5/14(-). The relay should trip with a target of SBP. Change jumpers from JMP 7 and 9 back to JMP 8 and 10; if the Stub Bus Protection is not used. Reset CIF to "NO".

2.1.4 Input Transformer (I_P) Check

Step 9. Change the settings from Table H-1 (or Table H-3) as follows:

ZIP = OUT
ZIG = OUT
DIRU = DUAL
GBCV = CO-8
GBPU = 0.5
GDIR = YES
GTC = 24

For a dual polarizing ground directional unit (DIRU = DUAL) test, connect the test circuit shown in **Figure H-4**. Apply I_P = 1.0A ∠–90° to terminals 12(+) and 11(-), and apply a balanced 3-phase voltage (70 Vac) to Va, Vb, Vc, and Vn. Apply Ia = 4A to terminals 6 (+) and 5 (-). The relay should trip at the following angles:

- -3°
- -90° (± 87°)
- -177°

The relay should *not* trip at the following angles:

- +3°
- +90° (± 87°)
- +177°

Change the settings back to Table H-1.

2.1.5 Output Contact Test

Step 10. The purpose of this test is to check the hardware connections and relay contacts. It is designed for a bench test only. Remove JMP12 (spare on the Microprocessor PC Board) and place it in the JMP 5 position.

Change the LED mode to "TEST" and select the tripping function field and the desired contact in the value field. Push the ENTER button; the ENTER LED should be "ON". The corresponding relay should operate when the ENTER button is pressed. The following contacts can be tested:

- TRIP
- BFI
- RI1 (optional)
- RI2
- RB
- AL1 (with 3 balanced voltages)
- AL2
- GS
- SEND (optional)
- STOP (optional)
- OC 1 to OC8 (Optional)

Remove JMP 5 and place it on JMP12.

2.2 PILOT MAINTENANCE TESt

Connect the MDAR per **Figure H-1**, Configuration 1.

2.2.1 Basic Function Test

Step 1. Repeat Step 1 thru 10 in the Non-Pilot Maintenance Test (2.1.1 thru 2.1.5).

2.2.2 Input Opto-Coupler Check

Step 2. PLT ENA Terminals

Change the following settings from Table H-1:

- PLT YES
- Z1P 0UT
- Z1G OUT
- PLTP OUT
- PLTG 6.0
- Z3P OUT
- Z3G 6.0
- T3P BLK
- T3G BLK
- Z3FR1 REV

a. Block Systems Only

Change the STYP setting to BLK. Apply a forward fault, as shown in the Non-Pilot Maintenance Test, step 5. The relay should not trip.

Apply a rated dc voltage to PLT ENA terminals TB 5/9(+) and TB 5/10(-). Repeat the test. The relay should trip.

b. POTT/PUTT Systems Only

Change the STYP setting to POTT. Change the LED mode to TEST and select the function “RS1”. Push the ENTER button; the LED should be “ON”. Apply a forward fault as shown in Non-Pilot Maintenance test, Step 5. With the ENTER button depressed, the relay should not trip. Apply a rated dc voltage to terminals TB 5/9(+) and TB 5/10(-). Repeat the test. The relay should trip.

Step 3. Receivers 1 and 2

Apply a dc voltage to PLT ENA terminals TB 5/9(+) and TB5/10(-).

a. Block Systems Only

Change the STYP setting to BLK. Apply a forward fault as shown in the Non-Pilot Maintenance test, Step 5. The relay should trip.

Apply a rated dc voltage to RCVR #1 terminals TB 5/7 (+) and TB 5/8(-). Repeat the test. The relay should not trip. Move the dc voltage from RCVR #1 to RCVR #2 terminals TB 5/11(+) and TB 5/12(-), and repeat this test for RCVR #2.

b. POTT/PUTT Systems Only

Change the STYP setting to POTT. Apply a forward fault as shown in the Non-Pilot Maintenance test, Step 5. The relay should not trip. Apply a rated dc voltage to RCVR #1 terminals TB 5/7(+) and TB 5/8(-). Repeat the test. The relay should trip.

Move the dc voltage from RCVR #1 to RCVR #2 terminals TB 5/11(+) and TB 5/12(-), and repeat this test for RCVR #2.

2.3 SINGLE-POLE TRIP TEST

2.3.1 Output Contact Test (Phases B and C)

Step 1. Set relay for Non-Pilot systems (Table H-1) or for Pilot systems (Table H-3). Check the 62T setting; it should be 5.000.

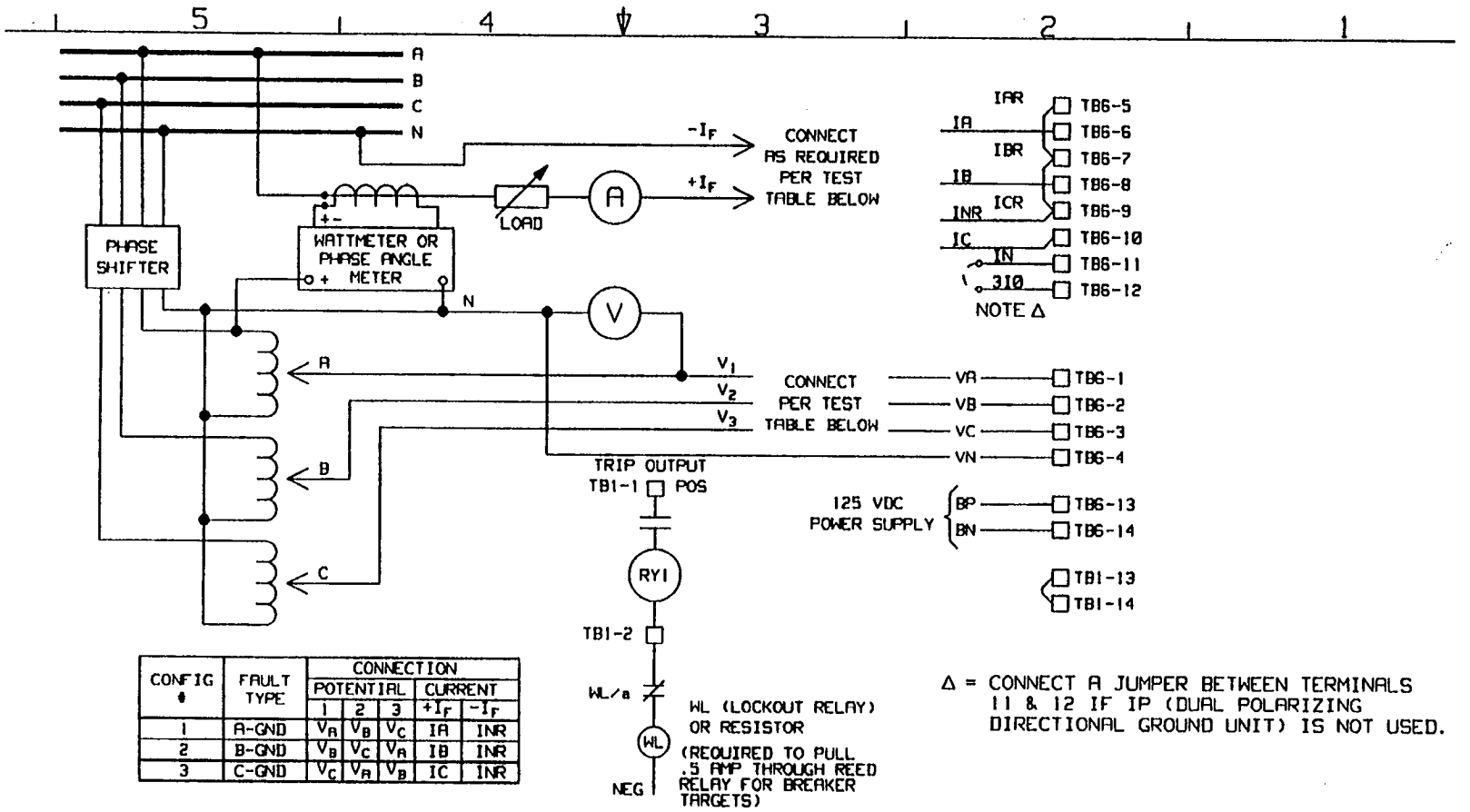
For a Pilot system, change the PLT setting to YES, and apply rated dc voltage to Pilot enable terminals TB 5/9(+) and TB 5/10(-). Also, apply a rated voltage to RCVR #1 terminals TB 5/7(+) and TB 5/8(-) if the STYP = POTT or PUTT; set TTYP = SPR.

Step 2. Repeat Non-Pilot Maintenance test, step 5 for trip and BFI. Check the contact closures for Trip A, Trip B, Trip C and BFIA, BFIB, BFIC.

2.3.2 Input Opto-Coupler Check

Step 3. 52a Terminals

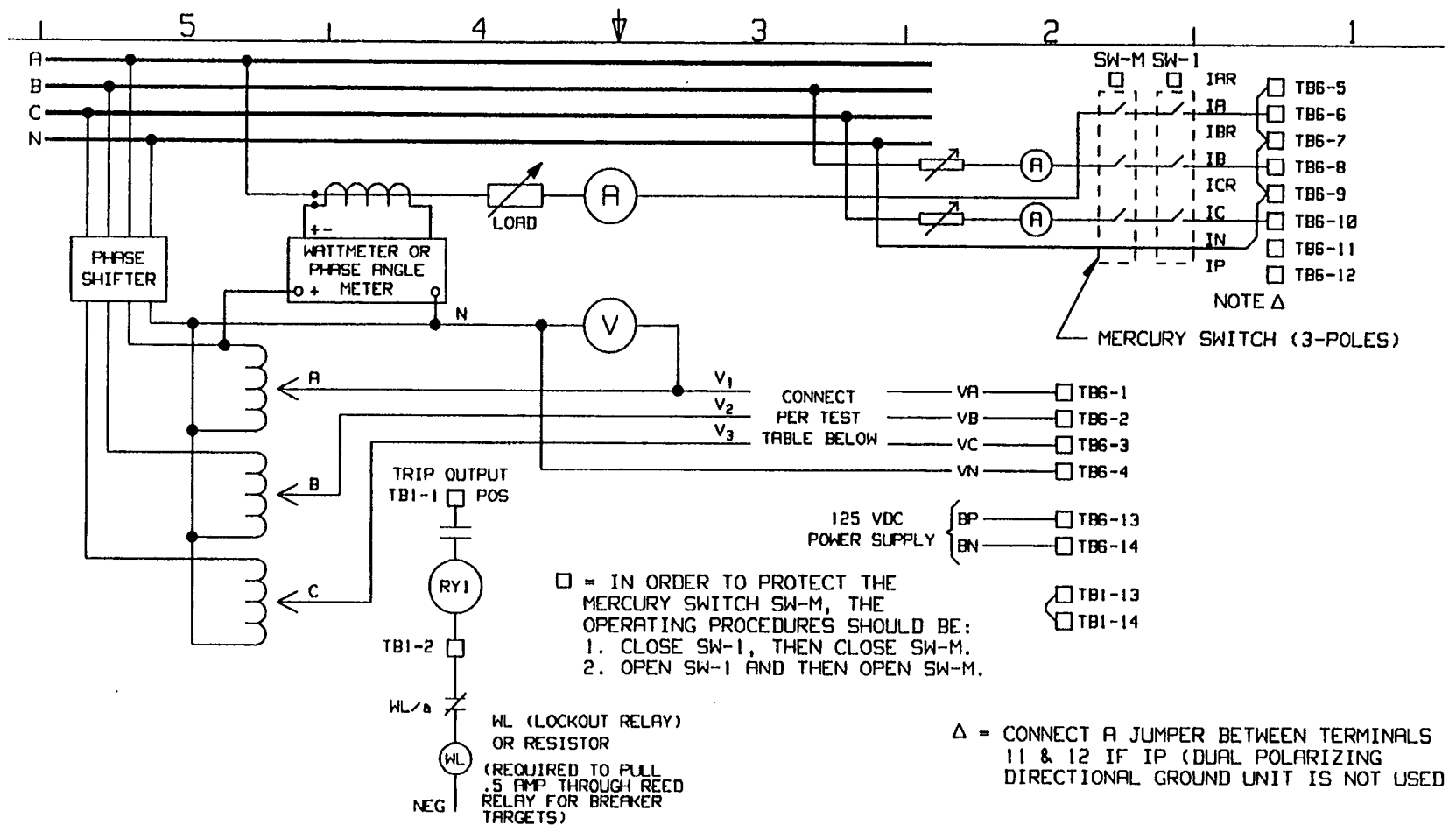
Apply a rated voltage to 52b terminals TB 5/3(+) and TB 5/4(-) and then apply a rated voltage to 52a terminals TB 5/1(+) and TB 5/2(-). The relay should trip in 5 seconds with a display of 62T.



CONFIG #	FAULT TYPE	CONNECTION				
		POTENTIAL			CURRENT	
		1	2	3	$+I_F$	$-I_F$
1	A-GND	V_A	V_B	V_C	IA	INR
2	B-GND	V_B	V_C	V_A	IB	INR
3	C-GND	V_C	V_A	V_B	IC	INR

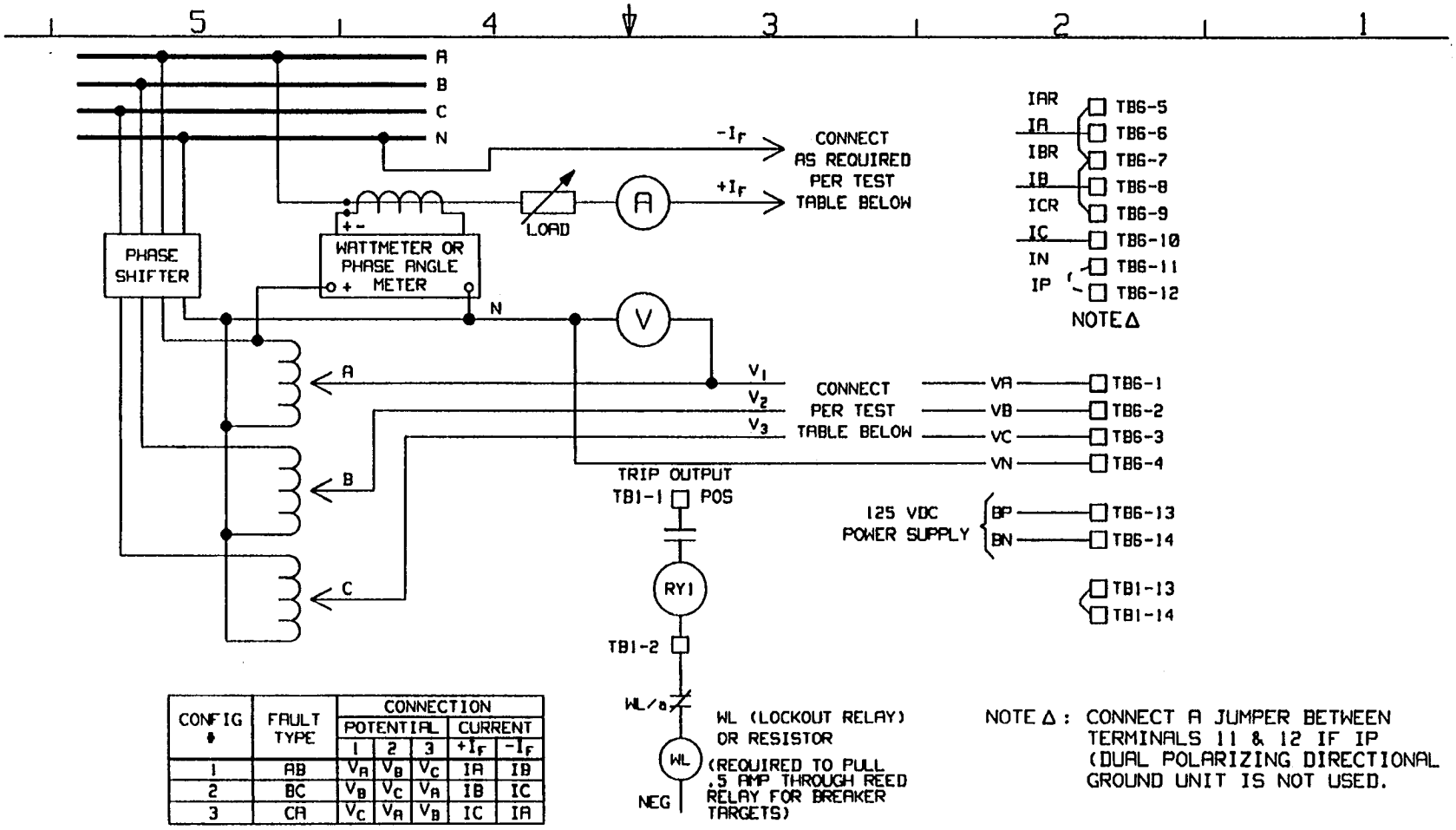
Sub 1
1502B51

Figure H-1 Test Connection for Single-Phase-to-Ground Faults (Sheet 1 of 4)



Sub 1
1502B51

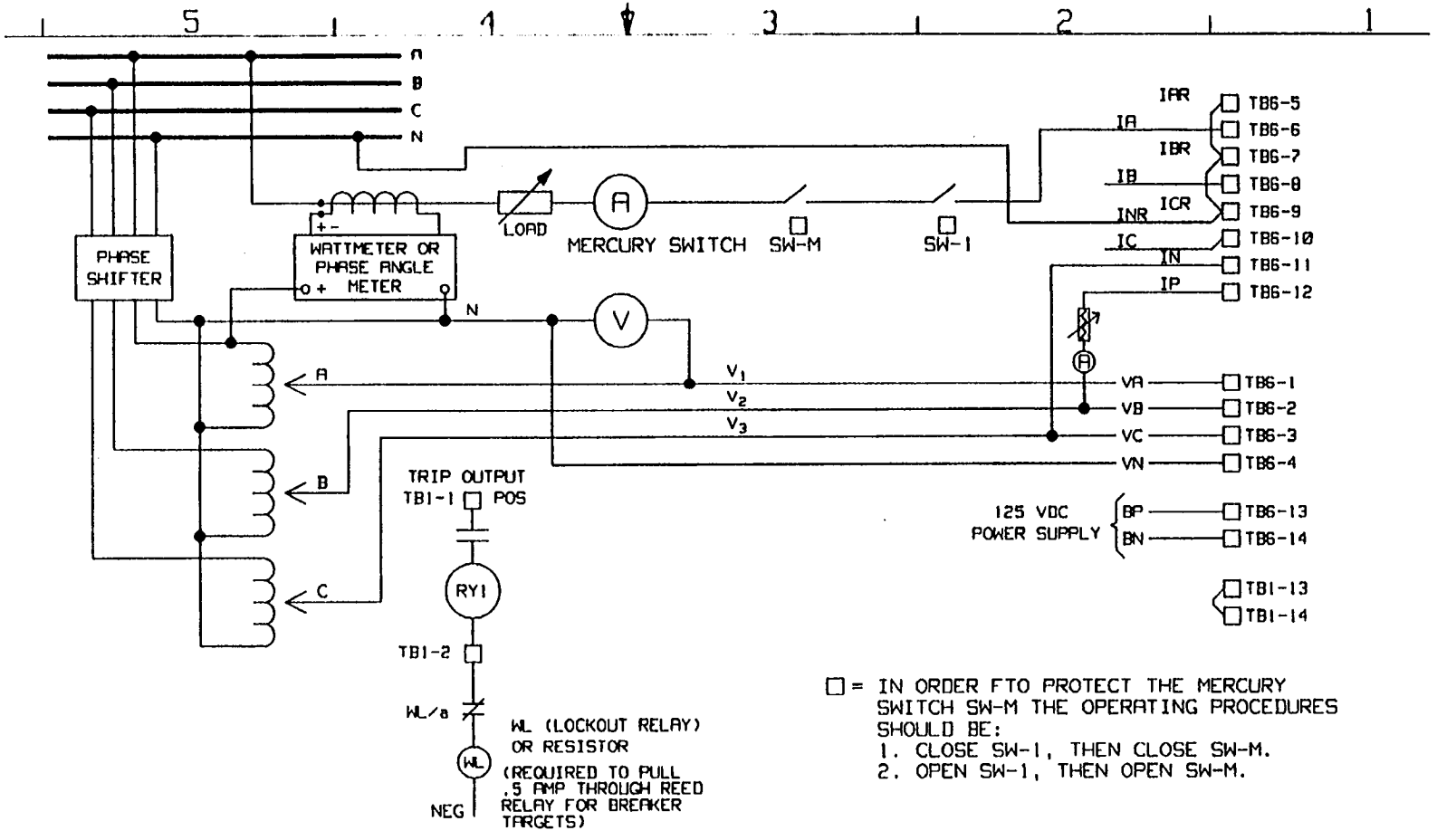
Figure H-2 Test Connection for Three-Phase Faults (Sheet 2 of 4)



CONFIG #	FAULT TYPE	CONNECTION				
		POTENTIAL			CURRENT	
		1	2	3	$+I_F$	$-I_F$
1	AB	V_A	V_B	V_C	IA	IB
2	BC	V_B	V_C	V_A	IB	IC
3	CA	V_C	V_A	V_B	IC	IA

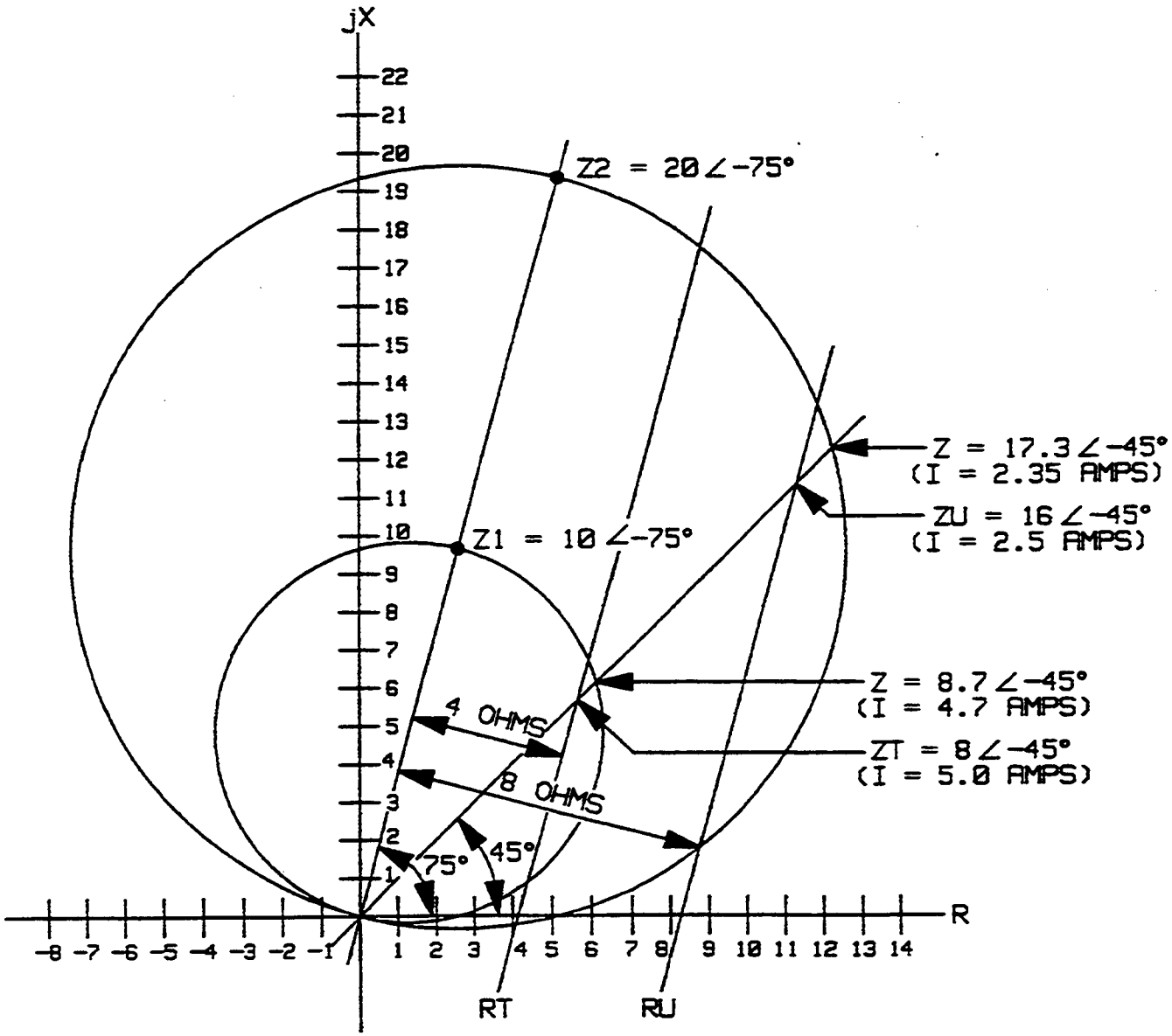
Sub 1
1502B51

Figure H-3 Test Connection for Phase-to-Phase Faults (Sheet 3 of 4)



Sub 1
1502B51

Figure H-4 Test Connection for Dual Polarizing Ground Directional Unit (Sheet 4 of 4)



INPUTS: Va = 40∠0°, Vb = 40∠-120°, Vc = 40∠120°
SETTINGS: PANG = 75°, GANG = 75°, ZR = 3
ABC FAULT WITH FAULT ANGLE OF 45°

Sub 1
9651A71

Figure H-5 MDAR with Out-of-Step Block Option

TABLE H-1. PRESENT MDAR SETTINGS (PILOT SYSTEM) – V2.1x

VERS	0	Z3P	OUT
OSC	TRIP	T3P	2.00
FDAT	TRIP	Z3G	OUT
CTR	1000	T3G	2.50
VTR	2000	Z3FR	FWD
FREQ	60	PANG	75
CTYP	5	GANG	75
RP	NO	ZR	3.0
XPUD	.5	LV	60
DTYP	KM	IL	.5
TTYP	OFF	IM	1.0
62T	5.000*	IOS	.5
Z1RI	YES	IOM	1.0
Z2RI	NO	ITP	OUT
Z3RI	NO	ITG	OUT
BFRB	NO	OSB	NO
PLT	NO	OSOT	4000
STYP	3ZNP	RT	15.00
FDGT	0	RU	15.00
WFEN	NO	DIRU	ZSEQ
3TRM	NO	GBCV	OUT
BLKT	0	GBPU	.5
PLTP	OUT	GTC	24
PLTG	6.00	GDIR	YES
Z1P	4.5	CIF	NO
Z1G	4.5	LLT	NO
T1	NO	LOPB	NO
Z2P	OUT	LOIB	NO
T2P	1.00	AL2S	NO
Z2G	OUT	SETR	YES
T2G	1.50	TIME	NO

* For Single Pole Trip option only.

NOTE: This MDAR settings table is for 60 Hz and 5A ct systems. For 1A ct, change PLT, PLG, Z1P, Z1G, Z2P, Z2G, Z3P, Z3G, RT, RU by multiplying a factor of 5, and all current values mentioned in the text should be multiplied by a factor of 0.02.

TABLE H-2. TRIP TIME CONSTANTS FOR CO CURVES

Curve #	T_0	K	C	P	R
CO2	111.99	735.00	0.675	1	501
CO5	8196.67	13768.94	1.13	1	22705
CO6	784.52	671.01	1.19	1	1475
CO7	524.84	3120.56	0.08	1	2491
CO8	477.84	4122.08	1.27	1	9200
CO9	310.01	2756.06	1.35	1	9342
CO11	110.	17640.00	0.5	2	8875

TABLE H-1. PRESENT MDAR SETTINGS (PILOT SYSTEM) – V2.1x

VERS	0	Z3P	OUT
OSC	TRIP	T3P	2.00
FDAT	TRIP	Z3G	OUT
CTR	1000	T3G	2.50
VTR	2000	Z3FR	FWD
FREQ	60	PANG	75
CTYP	5	GANG	75
RP	NO	ZR	3.0
XPUD	.5	LV	60
DTYP	KM	IL	.5
TTYP	OFF	IM	1.0
62T	5.000*	IOS	.5
Z1RI	YES	IOM	1.0
Z2RI	NO	ITP	OUT
Z3RI	NO	ITG	OUT
BFRB	NO	OSB	NO
PLT	NO	OSOT	4000
STYP	3ZNP	RT	15.00
FDGT	0	RU	15.00
WFEN	NO	DIRU	ZSEQ
3TRM	NO	GBCV	OUT
BLKT	0	GBPU	.5
PLTP	OUT	GTC	24
PLTG	6.00	GDIR	YES
Z1P	4.5	CIF	NO
Z1G	4.5	LLT	NO
T1	NO	LOPB	NO
Z2P	OUT	LOIB	NO
T2P	1.00	AL2S	NO
Z2G	OUT	SETR	YES
T2G	1.50	TIME	NO

* For Single Pole Trip option only.

NOTE: This MDAR settings table is for 60 Hz and 5A ct systems. For 1A ct, change PLT, PLG, Z1P, Z1G, Z2P, Z2G, Z3P, Z3G, RT, RU by multiplying a factor of 5, and all current values mentioned in the text should be multiplied by a factor of 0.02.

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CO5	8196.67	13768.94	1.13	1	22705
CO6	784.52	671.01	1.19	1	1475
CO7	524.84	3120.56	0.08	1	2491
CO8	477.84	4122.08	1.27	1	9200
CO9	310.01	2756.06	1.35	1	9342
CO11	110.	17640.00	0.5	2	8875

TABLE H-3. FAULT TYPES APPLIED TO MDAR

SETTING TTYP	FAULT TYPE APPLIED	OUT CONTACTS RI	TRIP	BFI
OFF	AG	NO	A,B,C	A,B,C
	BG	NO	A,B,C	A,B,C
	CG	NO	A,B,C	A,B,C
	ABC	NO	A,B,C	A,B,C
1PR	AG	RI2	A,B,C	A,B,C
	AB	NO	A,B,C	A,B,C
	ABC	NO	A,B,C	A,B,C
2PR	AG	RI2	A,B,C	A,B,C
	AB	RI2	A,B,C	A,B,C
	ABC	NO	A,B,C	A,B,C
3PR	AG	RI2	A,B,C	A,B,C
	BG	RI2	A,B,C	A,B,C
	CG	RI2	A,B,C	A,B,C
	AB	RI2	A,B,C	A,B,C
	ABC	RI2	A,B,C	A,B,C
SPR	AG	RI1	A	A
	BG	RI1	B	B
	CG	RI1	C	C
	ABC	NO	A,B,C	A,B,C
SR3R	AG	RI1	A	A
	BG	RI1	B	B
	CG	RI1	C	C
	ABC	RI2	A,B,C	A,B,C

Appendix J. System Diagrams

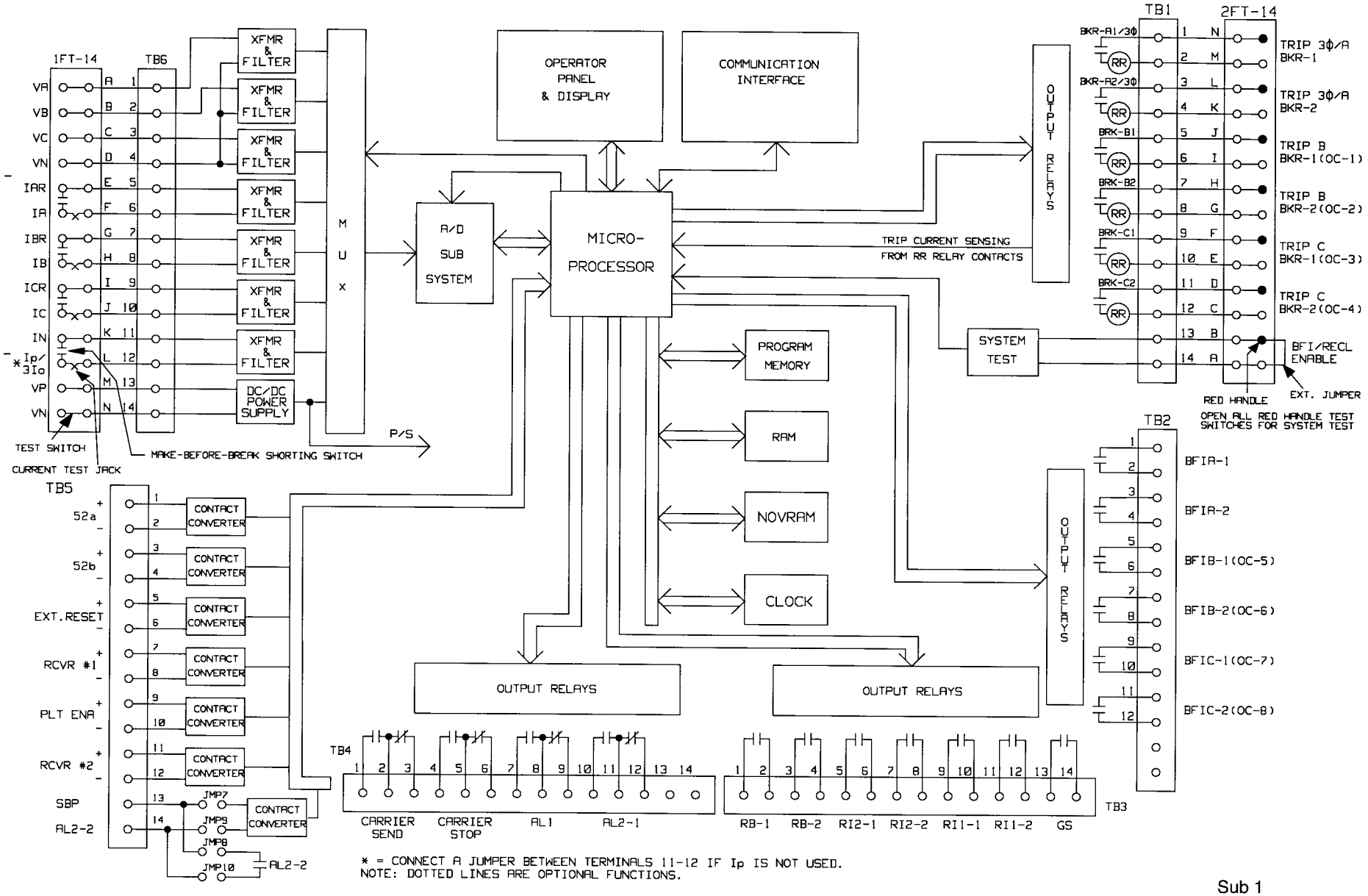
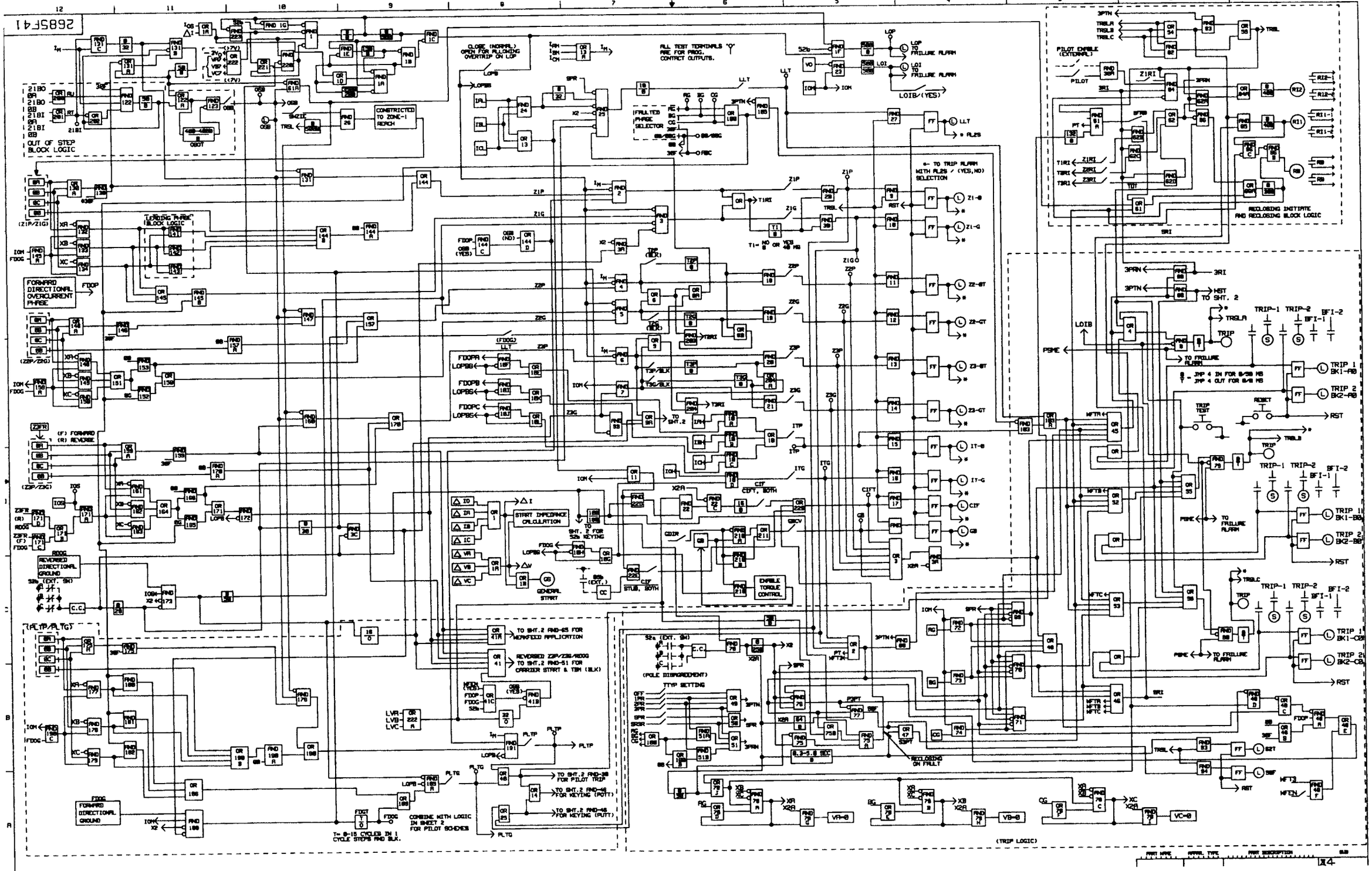
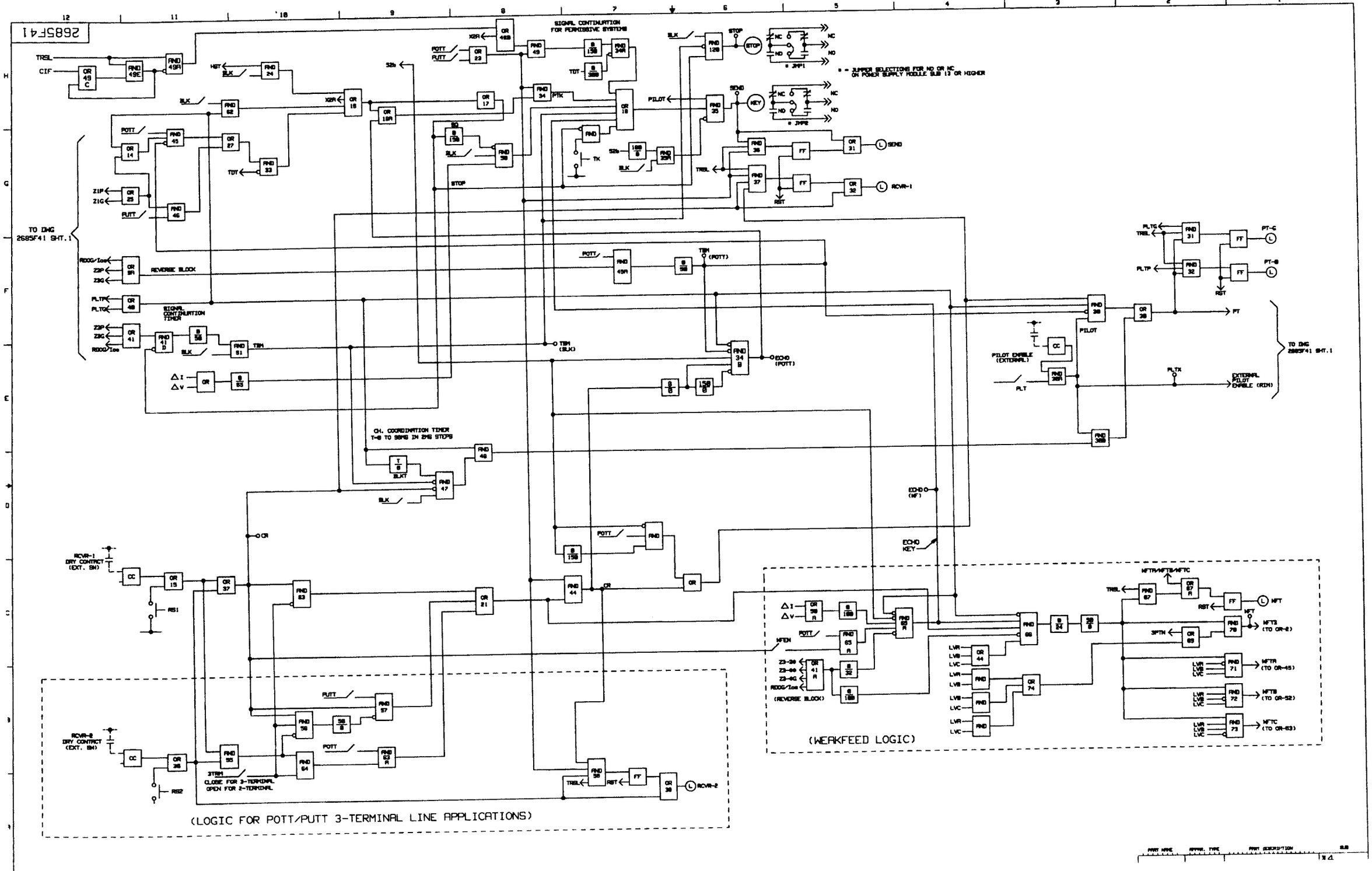
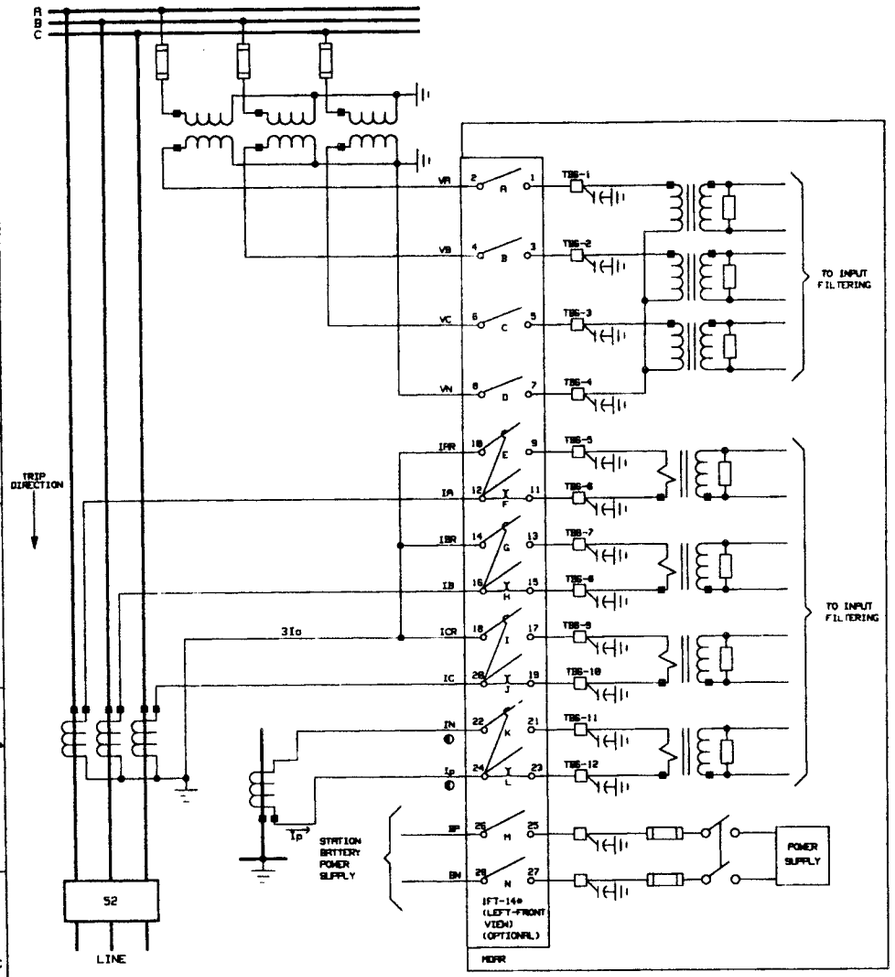
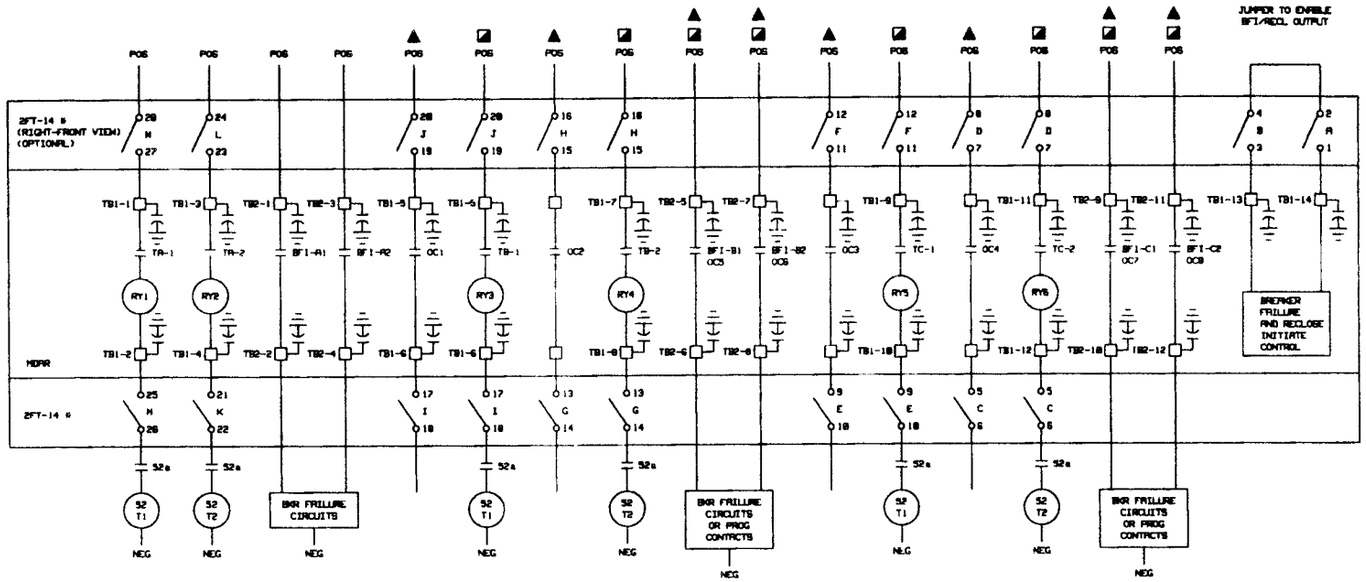


Figure J-1. MDAR Block Diagram


OUT OF STEP BLOCK LOGIC
FORWARD DIRECTIONAL OVERCURRENT PHASE
REVERSED DIRECTIONAL GROUND
FDOG FORWARD DIRECTIONAL GROUND
START IMPEDANCE CALCULATION
GENERAL START
ENABLE TORQUE CONTROL
CONSTRICTED TO ZONE-1 REACH
ALL TEST TERMINALS ARE FOR PROG. CONTACT OUTPUTS.
CLOSE (NORMAL) OPEN FOR ALLOWING OVERTRIP ON LOP
LOP TO FAILURE ALARM
LOI TO FAILURE ALARM
LOIB/(YES)
FAULTED PHASE SELECTOR
← TO TRIP ALARM WITH ALPS / (YES,NO) SELECTION
PILOT ENABLE (EXTERNAL)
RECLOSING INITIATE AND RECLOSING BLOCK LOGIC
TRIP TEST
RESET
TRIP-1 TRIP-2 BFI-1 BFI-2
TO FAILURE ALARM
TO SHT. 2
TO SHT. 2 FOR 52b KEYING
TO SHT.2 FOR MEMFEED APPLICATION
REVERSED Z2P/Z3G/RDOG TO SHT.2 FOR CARRIER START & TBK (BLK)
TO SHT.2 FOR PILOT TRIP
TO SHT.2 FOR KEYING (POTT)
TO SHT.2 FOR KEYING (PUTT)
COMBINE WITH LOGIC IN SHEET 2 FOR PILOT SCHEMES
T= 8-15 CYCLES IN 1 CYCLE STEPS AND BLK.
(POLE DISAGREEMENT)
TYYP SETTING
RECLOSING ON FAULT
(TRIP LOGIC)
PART NAME
PANEL TYPE
PART DESCRIPTION

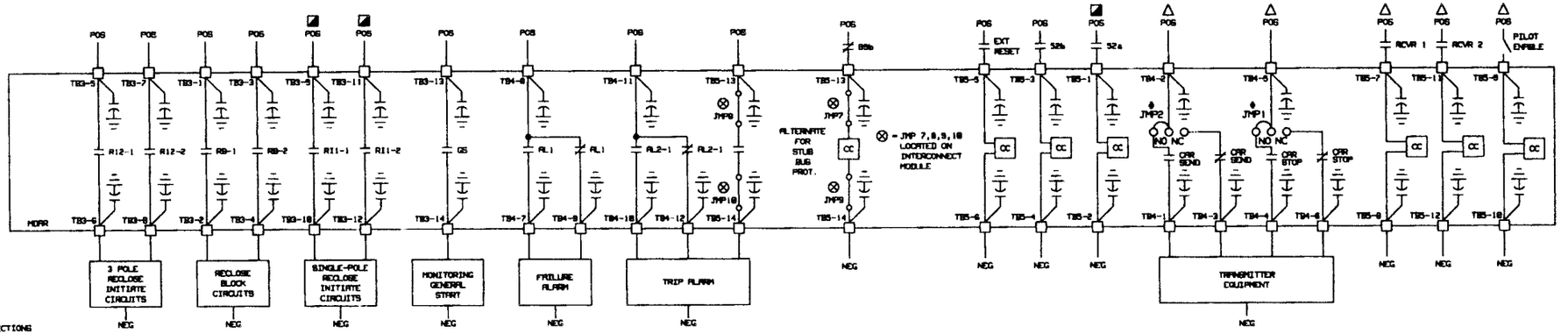

2685F41
SIGNAL CONTINUATION FOR PERMISSIVE SYSTEMS
* = JUMPER SELECTIONS FOR NO OR NC ON POWER SUPPLY MODULE SUB 13 OR HIGHER
TO DWG 2685F41 SHT. 1
REVERSE BLOCK
SIGNAL CONTINUATION TIMER
CH. COORDINATION TIMER T=8 TO 98MS IN 2MS STEPS
PILOT ENABLE (EXTERNAL)
EXTERNAL PILOT ENABLE (RIM)
ECHO (POTT)
ECHO (MF)
ECHO KEY
RCVR-1 DRY CONTACT (EXT. SW)
RCVR-2 DRY CONTACT (EXT. SW)
3TRM CLOSE FOR 3-TERMINAL OPEN FOR 2-TERMINAL
(LOGIC FOR POTT/PUTT 3-TERMINAL LINE APPLICATIONS)
(WEAKFEED LOGIC)
(REVERSE BLOCK)





LEGEND:

- ◪ = CONNECTIONS FOR USE WITH SINGLE-POLE TRIP OPTION ONLY.
- △ = CONNECTIONS FOR USE WITH PILOT TRIP OPTION ONLY.
- ✳ = FT-14 SWITCH SUPPLIED AS OPTION. WHEN NOT SUPPLIED, CONNECTIONS SHOULD BE MADE TO CORRESPONDING TB1 AND TB2 TERMINAL BLOCKS.
- ◐ = CONNECT A JUMPER BETWEEN TERMINALS 22 & 24 IF Ip IS NOT USED.
- ▲ = CONNECTIONS FOR USE WITH PROGRAMMABLE CONTRACT OPTION ONLY. JUMPERS JMP1 TO 4 ON THE CONTACT MODULE FOR THE SELECTION OF NO OR NC CONTACTS OF OC5, 6, 7 & 8, RESPECTIVELY.
- ♦ = JUMPER SELECTIONS FOR NO OR NC ON POWER SUPPLY MODULE SUB 13 OR HIGHER



INPUT/OUTPUT EXTERNAL CONNECTIONS

Appendix I. Index/Glossary of Nomanclature

Numerics

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