SIEMENS

Numerical Paralleling Device

7VE51 V1.7

Instruction Manual Order No. C53000–G1176–C80–7

Figure 1 Illustration of the numerical paralleling device 7VE512 (in flush mounting case)

SIEMENS

CE

Conformity

This product is in conformity with the directive of the Council of the European Communities on the approximation of the laws of the Member States relating to electromagnetic compatibility (EMC Council Directive 89/336/EEC) and concerning electrical equipment for application within specified voltage limits (Low−voltage directive 73/23 EEC).

Conformity is proved by tests that had been performed according to article 10 of the Council Directive in accordance with the generic standards EN 50081−2 and EN 50082−2 (for EMC directive) and the standards EN 60255−6 (for low−voltage directive) by Siemens AG.

The device is designed and manufactured for application in industrial environment.

The device is designed in accordance with the international standards of IEC 255 and the German standards DIN 57 435 part 303 (corresponding to VDE 0435 part 303).

Contents

NOTE:

This instruction manual does not purport to cover all details in equipment, nor to provide for every possible contingency to be met in connection with installation, operation or maintenance.

Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purpose, the matter should be referred to the local Siemens sales office.

The contents of this instruction manual shall not become part nor modify any prior or existing agreement, commitment or relationship. The sales contract contains the entire obligations of Siemens. The warranty contained in the contract between the parties is the sole warranty of Siemens. Any statements contained herein do not create new warranties nor modify the existing warranty.

1 Introduction

1.1 Application

The numerical paralleling device 7VE51 is suitable for paralleling generators with networks and for paralleling networks which are already synchronous.

Several synchronize locations can be operated from one device by remote selection of various setting parameter blocks.

The model 7VE511 has all functions required for synchronous or asynchronous paralleling. It has two isolated binary inputs and two setting parameter blocks and is thus suitable for two remote selection locations.

The model 7VE512 additionally contains voltage and frequency balancers whose working ranges and control commands can be individually matched to the properties of the generator and of the voltage and speed regulators. Thus completely automatic synchronization of generators with the network is possible. This model has a total of six isolated binary inputs and six setting blocks for six remote selection locations. The balancing outputs can be replaced by status signals which indicate the status of the voltages, frequencies, and angle difference.

The high safety and availability of the device are guaranteed by two analog input circuits with separate measured value inputs and analog–to–digital converter ranges, two different and logically independent methods of measurement, two command relays controlled by different criteria, together with comprehensive monitoring functions and plausibility checks.

1.2 Features

- Processor system with powerful 16–bit microprocessor;
- Complete digital measured value processing and control from data acquisition and digitizing of the measured values up to the output of status signals, control and close commands;
- Complete galvanic and reliable separation of the internal processing circuits from the measurement, control and supply circuits of the system, with screened input transducers, binary input and output modules and d.c./d.c. converter;
- Dual channel design of measured value processing with two different and logically independent methods;
- Applicable for paralleling of synchronous and asynchronous networks as well as for synchronizing of generators with networks, optionally with voltage and frequency balancer;
- Remote switch–over of setting parameter blocks for use on several different paralleling locations possible;
- Calculation of operational measured values and indication on the front display;
- Simple setting and operation using the integrated operation panel or a connected personal computer with menu–guided software;
- Storage of indication;
- Continuous monitoring of the hardware and software of the device.

2 Design

2.1 Arrangements

Depending on the application, two basic models are available:

For paralleling asynchronous or synchronous voltage sources with **two** selectable parameter blocks 7VE511

For paralleling asynchronous or synchronous voltage sources with **six** selectable parameter blocks, with frequency and voltage balancer 7VE512

In the 7VE511, all functions including dc/dc converter are accommodated on one basic plug−in module of Double Europa Format. In the 7VE512, an additional plug−in module is added to the basic module. In the following the data applying to the 7VE512 are given in ( ) should they deviate from the 7VE511 model.

The modules are installed in a housing 7XP20. Two different types of housings can be delivered:

– **7VE51⋆⋆−⋆D⋆⋆⋆−** in housing 7XP2030−1 (7XP2040−1) for **panel surface mounting**

  The housing has full sheet−metal covers, as well as a removable front cover with transparent plastic window.

  Plastic guide rails are built in for the support of plug−in modules. Next to the guide rail at the bottom on the left−hand side of each module, a contact area which is electrically connected to the housing is installed to mate with the earthing spring of the module. Connection to earth is made before the plugs make contact. Earthing screws have been provided on the left hand side of the housing. Additionally, terminal 16 (26) is connected to the case.

  All external signals are connected to 60 (100) screwed terminals which are arranged over cut−outs on the top and bottom covers. The terminals are numbered consecutively from left to right at the bottom and top.

  The degree of protection for the housing is IP51, for the terminals IP21. For dimensions please refer to Figure 2.2 (2.4).

– **7VE51⋆⋆−⋆C⋆⋆⋆−** in housing 7XP1030−2 (7XP2040−2) for **panel flush mounting** or **7VE51⋆⋆−⋆E⋆⋆⋆−** for **cubicle installation**

  The housing has full sheet−metal covers, as well as a removable front cover with transparent plastic window for panel mounting.

  Plastic guide rails are built in for the support of plug−in modules. Next to the guide rail at the bottom on the left−hand side of each module, a contact area which is electrically connected to the housing is installed to mate with the earthing spring of the module. Connection to earth is made before the plugs make contact. Earthing screws have been provided on the rear wall of the housing.

  All external signals are connected to connector modules which are mounted on the rear cover over cut−outs. For each electrical connection, one screwed terminal and one parallel snap−in terminal are provided. For field wiring, the use of the screwed terminals is recommended; snap−in connection requires special tools.

  The plug modules are labelled according to their mounting position by means of a grid system (e.g. **1A**4). The individual connections within a module are numbered consecutively from left to right (when viewed from the rear), (e.g. 1A**4**); refer to Figure 2.1.

  Degree of protection for the housing is IP51 (for cubicle installation IP30), for the terminals IP21. For dimensions please refer to Figure 2.3 (2.5).

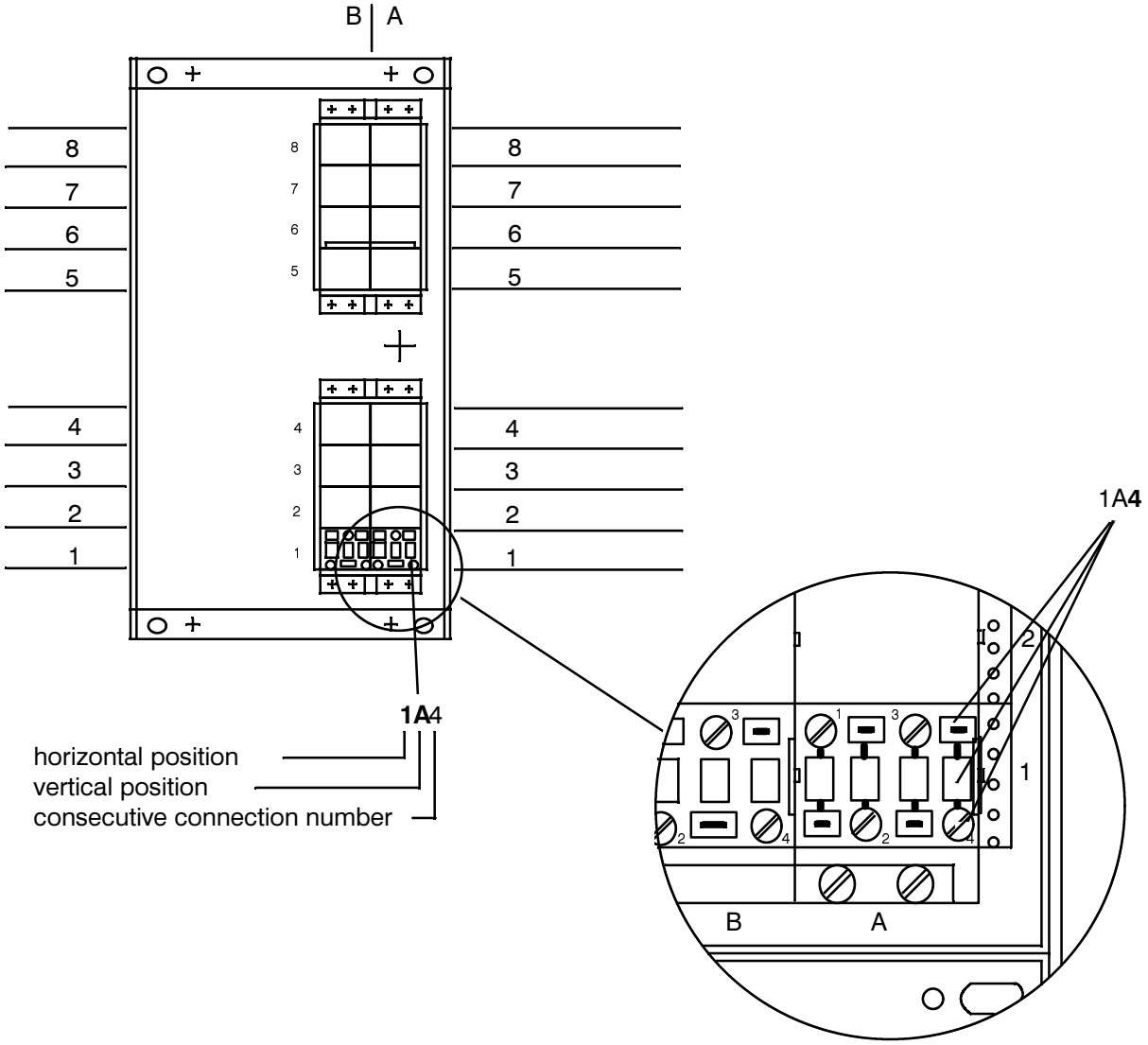
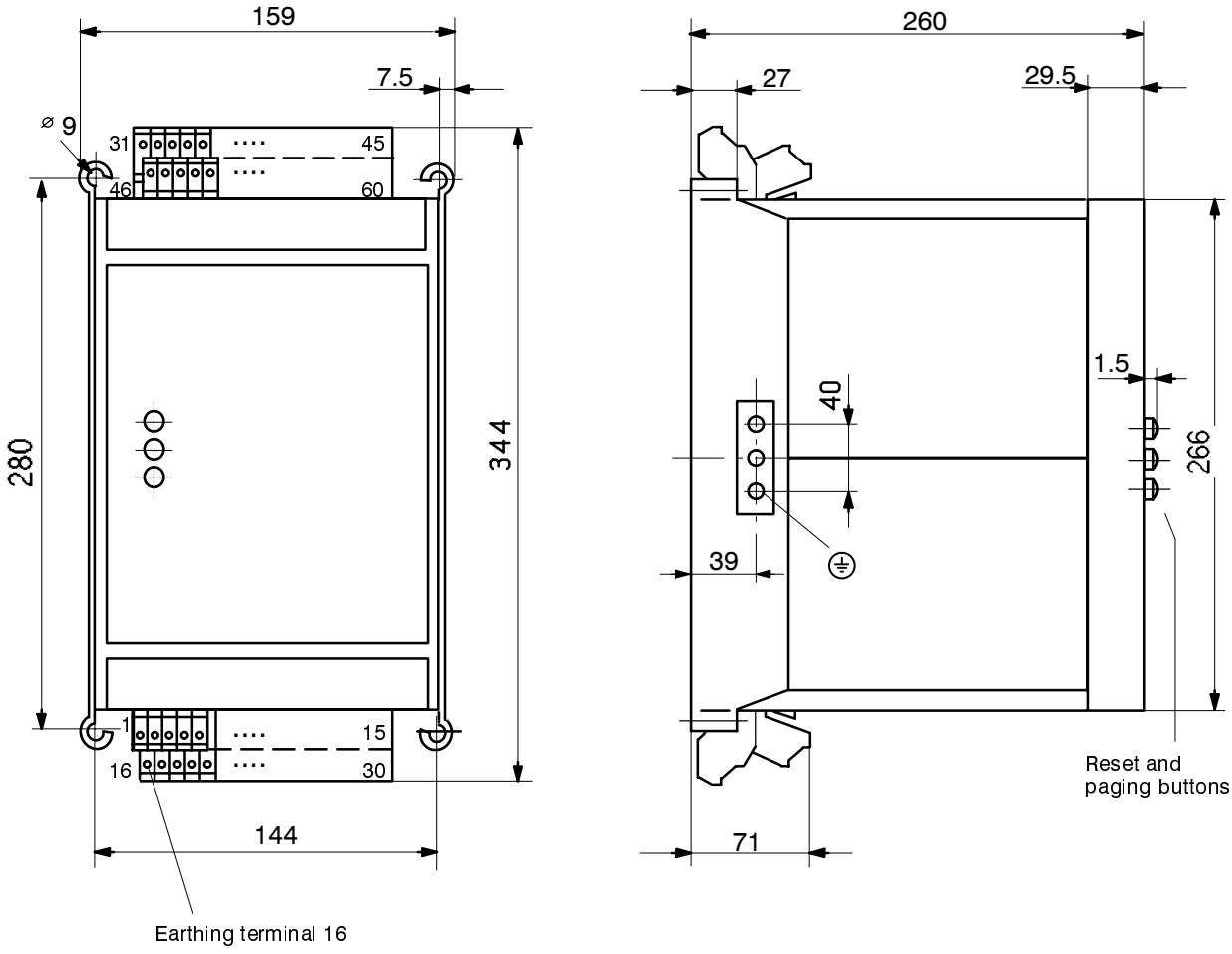


Figure 2.1 Connection plugs (rear view) – housing for flush mounting – example

2.2 Dimensions

Figures 2.2 to 2.5 show the dimensions of the various types of housings available.

7VE511 Housing for **panel surface mounting** 7XP2030−1



Max. 60 terminals for cross−section max. 7 mm^2

Dimensions in mm

Figure 2.2 Dimensions for housing 7XP2030−1 for panel surface mounting

7VE511 Housing for **panel flush mounting** or **cubicle installation** 7XP2030−2

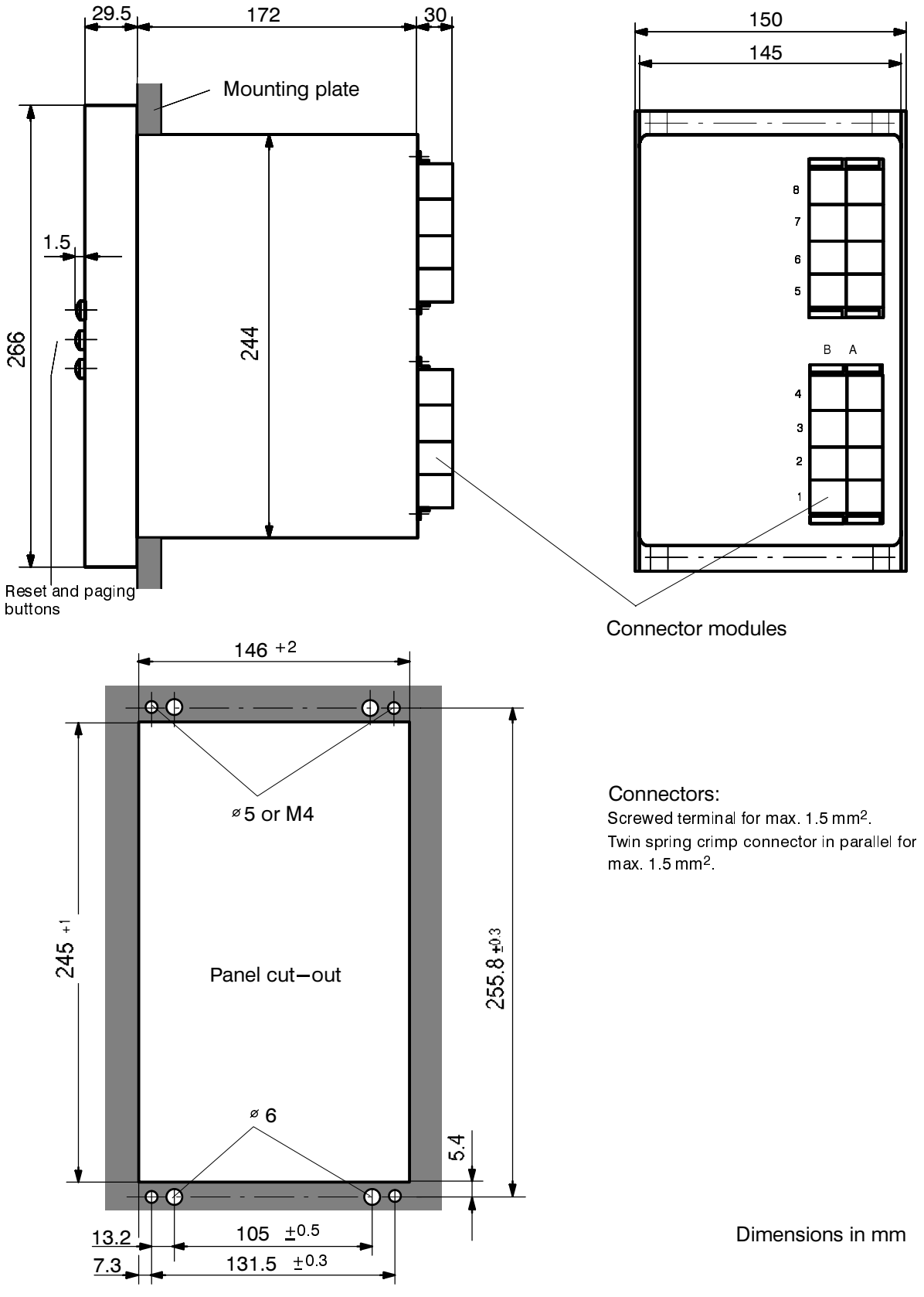
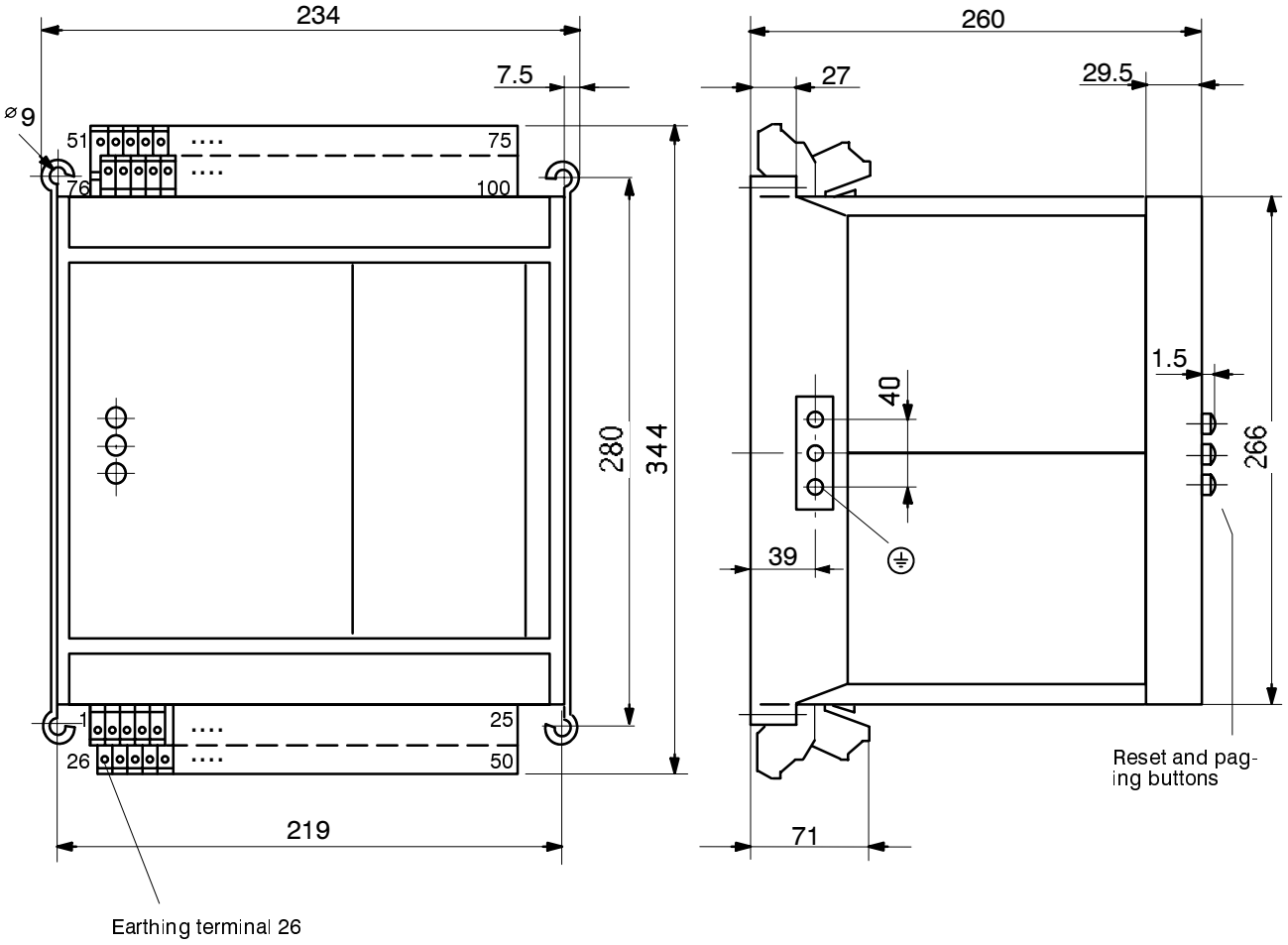


Figure 2.3 Dimensions for housing 7XP2030−2 for panel flush mounting or cubicle installation

7VE512 Housing for **panel surface mounting** 7XP2040−1

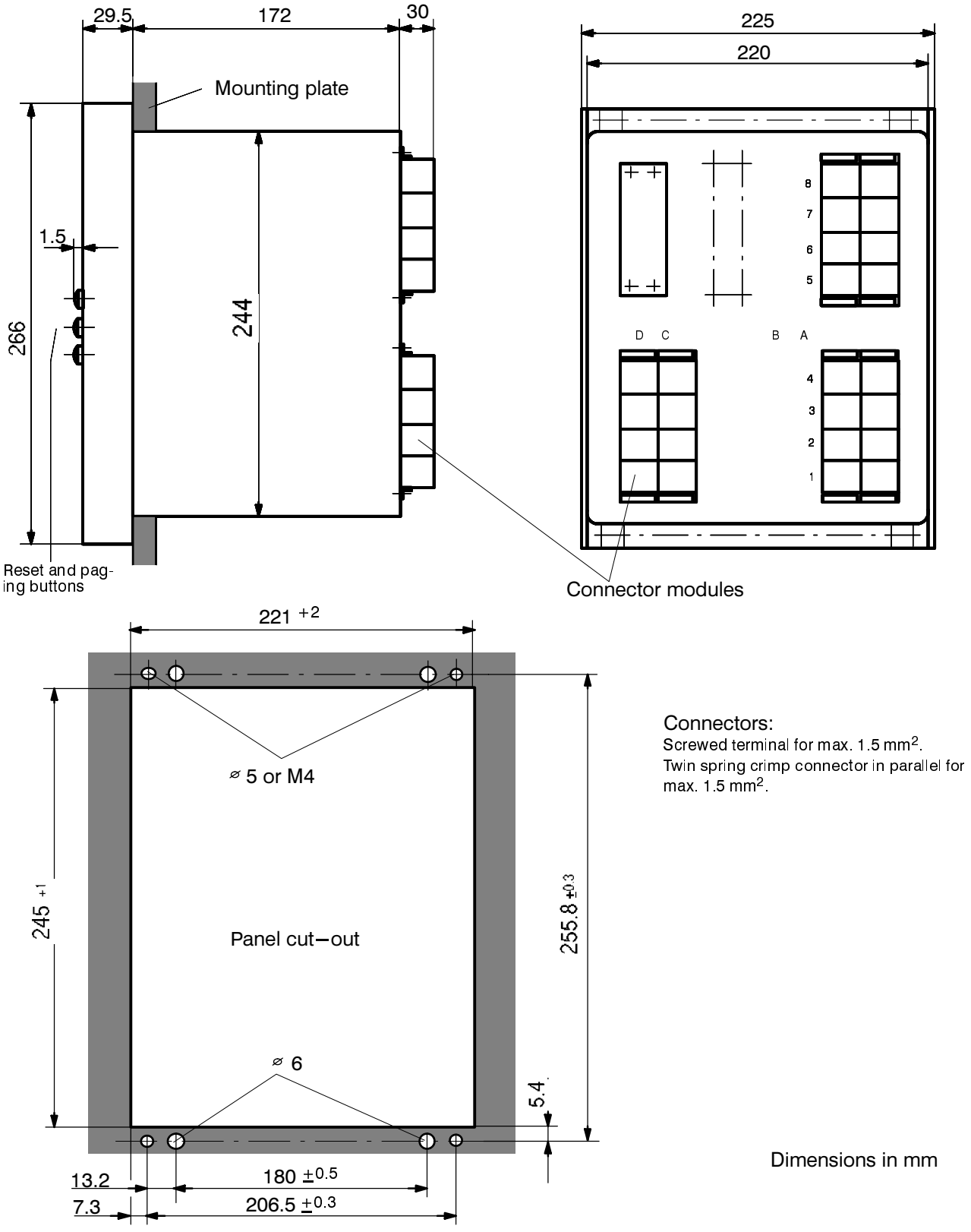


Max. 100 terminals for cross−section max. 7 mm^2

Dimensions in mm

Figure 2.4 Dimensions for housing 7XP2040−1 for panel surface mounting

7VE512 Housing for **panel flush mounting** or **cubicle installation** 7XP2040−2



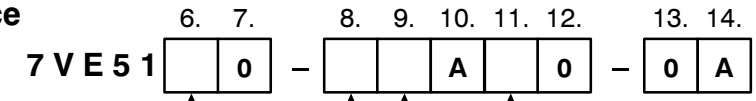
Connectors:
Screwed terminal for max. 1.5 mm^2.
Twin spring crimp connector in parallel for max. 1.5 mm^2.

Dimensions in mm

Figure 2.5 Dimensions for housing 7XP2040−2 for panel flush mounting or cubicle installation

2.3 Ordering data

Numerical Paralleling Device



Paralleling of asynchronous and synchronous voltage sources
2 selectable parameter sets 1

Paralleling of asynchronous and synchronous voltage sources
6 selectable parameter sets
frequency and voltage balancer 2

Auxiliary voltage

24/48 V dc 2

60/110/125 V dc 4

220/250 V dc 5

Construction

in housing 7XP20 for panel surface mounting . . . . . D

in housing 7XP20 for panel flush mounting C

in housing 7XP20 for cubicle installation (without glass window) . . . E

English operation language, f_N = 50 Hz/60 Hz 1

3 Technical data

3.1 General data

3.1.1 Inputs/outputs

Measuring circuits

Rated voltage U_N	100 V to 125 V
Voltage operation range	40 V to 130 V
Rated frequency f_N	50/60 Hz (settable)
Frequency operation range f1	f_N−2.5 Hz to f_N+2.5 Hz for f_N = 50 Hz f_N−3 Hz to f_N+3 Hz for f_N = 60 Hz
Power consumption at 100 V	<0.6 VA per measured value input
Overload capability, thermal	140 V ac continuous

Auxiliary voltage

Power supply via integrated dc/dc converter

Rated auxiliary voltage U_H	24/48 Vdc	60/110/125 Vdc	220/250 Vdc
Permissible variations	19 to 56 Vdc	48 to 144 Vdc	176 to 288 Vdc

Superimposed ac voltage, peak−to−peak	≦12 % at rated voltage ≦ 6 % at limits of admissible voltage

Power consumption	7VE511	7VE512
quiescent	approx. 9 W	approx. 10 W
energized	approx. 11 W	approx. 15 W

Bridging time during failure/short−circuit of auxiliary voltage	≧ 50 ms at U_{rated} ≧ 110 Vdc

Heavy duty (command) contacts

Closing contacts		4 NO
Switching capacity	MAKE	1000 W/VA
	BREAK	30 W/VA
Switching voltage		250 V
Permissible current		5 A continuous
		30 A for 0.5 s

Control contacts

for frequency and voltage balancer	in 7VE512 only
number	4 NO (f↑, f↓, U↑, U↓)
Switching capacity MAKE/BREAK	20 W/VA
Switching voltage	250 V
Permissible current	1 A continuous

Signal contacts

number		3 in 7VE511, 6 in 7VE512	
contacts per relay		1 CO or 1 NO (refer to general diagram Appendix A)	
Switching capacity	MAKE/BREAK	20	W/VA
Switching voltage		250	V
Permissible current		1	A

Binary inputs, number — 4 in 7VE511, 8 in 7VE512

Operating voltage	24 to 250 Vdc
Current consumption	approx. 1.7 mA, independent of operating voltage

Serial interface

Operator terminal interface	non−isolated
− Connection	at the front, 25−pole subminiature connector ISO 2110 for connection of a personal computer

3.1.2 Electrical tests

Insulation tests	
Standards:	IEC 255−5
− High voltage test (routine test) except d.c. voltage supply input	2 kV (rms); 50 Hz
− High voltage test (routine test) only d.c. voltage supply input	2.8 kV dc
− Impulse voltage test (type test) all circuits, class III	5 kV (peak); 1.2/50 μs; 0.5 J; 3 positive and 3 negative shots at intervals of 5 s
EMC tests; immunity (type tests)	
Standards:	IEC 255−6, IEC 255−22 (product standards) EN 50082−2 (generic standard) VDE 0435 /part 303
− High frequency IEC 255−22−1, class III	2.5 kV (peak); 1 MHz; τ =15 μs; 400 shots/s; duration 2 s
− Electrostatic discharge IEC 255−22−2 class III and IEC 1000−4−2, class III	4 kV/6 kV contact discharge; 8 kV air discharge; both polarities; 150 pF; R_i = 330 Ω
− Radio−frequency electromagnetic field, non−modulated; IEC 255−22−3 (report), class III	10 V/m; 27 MHz to 500 MHz
− Radio−frequency electromagnetic field, amplitude modulated; IEC 1000−4−3, class III	10 V/m; 80 MHz to 1000 MHz; 80 % AM; 1 kHz
− Radio−frequency electromagnetic field, pulse modulated; IEC 1000−4−3/ENV 50204, class III	10 V/m; 900 MHz; repetition frequency 200 Hz; duty cycle 50 %
− Fast transients IEC 255−22−4 and IEC 1000−4−4, class III	2 kV; 5/50 ns; 5 kHz; burst length 15 ms; repetition rate 300 ms; both polarities; R_i = 50 Ω; duration 1 min
− Conducted disturbances induced by radio−frequency fields, amplitude modulated IEC 1000−4−6, class III	10 V; 150 kHz to 80 MHz; 80 % AM; 1 kHz
− Power frequency magnetic field IEC 1000−4−8, class IV IEC 255−6	30 A/m continuous; 300 A/m for 3 s; 50 Hz 0.5 mT; 50 Hz
EMC tests; emission (type tests)	
Standard:	EN 50081−⋆ (generic standard)
− Conducted interference voltage, aux. voltage CISPR 22, EN 55022, class B	150 kHz to 30 MHz
− Interference field strength CISPR 11, EN 55011, class A	30 MHz to 1000 MHz

3.1.3 Mechanical stress tests

Vibration and shock during operation

Standards:	IEC 255−21 and IEC 68−2
− Vibration IEC 255−21−1, class 1 IEC 68−2−6	sinusoidal 10 Hz to 60 Hz: ± 0.035 mm amplitude; 60 Hz to 150 Hz: 0.5 g acceleration sweep rate 1 octave/min 20 cycles in 3 orthogonal axes
− Shock IEC 255−21−2, class 1	half sine acceleration 5 g, duration 11 ms, 3 shocks in each direction of 3 orthogonal axes
− Seismic vibration IEC 255−21−3, class 1 IEC 68−3−3	sinusoidal 1 Hz to 8 Hz: ± 3.5 mm amplitude (hor. axis) 1 Hz to 8 Hz: ± 1.5 mm amplitude (vert. axis) 8 Hz to 35 Hz: 1 g acceleration (hor. axis) 8 Hz to 35 Hz: 0.5 g acceleration (vert. axis) sweep rate 1 octave/min 1 cycle in 3 orthogonal axes

Vibration and shock during transport

Standards:	IEC 255−21 and IEC 68−2
− Vibration IEC 255−21−1, class 2 IEC 68−2−6	sinusoidal 5 Hz to 8 Hz: ± 7.5 mm amplitude; 8 Hz to 150 Hz: 2 g acceleration sweep rate 1 octave/min 20 cycles in 3 orthogonal axes
− Shock IEC 255−21−2, class 1 IEC 68−2−27	half sine acceleration 15 g, duration 11 ms, 3 shocks in each direction of 3 orthogonal axes
− Continuous shock IEC 255−21−2, class 1 IEC 68−2−29	half sine acceleration 10 g, duration 16 ms, 1000 shocks each direction of 3 orthogonal axes

3.1.4 Climatic stress tests

− Permissible ambient temperature

during service	−5 °C to +55 °C
during storage	−25 °C to +55 °C
during transport	−25 °C to +70 °C

Storage and transport with standard works packaging!

– Permissible humidity	mean value per year $\leq$ 75 % relative humidity; on 30 days per year 95 % relative humidity; Condensation not permissible!

We recommend that all units are installed such that they are not subjected to direct sunlight, nor to large temperature fluctuations which may give rise to condensation.

3.1.5 Service conditions

The relay is designed for use in industrial environment, for installation in standard relay rooms and compartments so that with proper installation **electro–magnetic compatibility (EMC)** is ensured. The following should also be heeded:

– All contactors and relays which operate in the same cubicle or on the same relay panel as the digital protection equipment should, as a rule, be fitted with suitable spike quenching elements.

– All external connection leads in sub–stations from 100 kV upwards should be screened with a screen capable of carrying power currents and earthed at both sides. No special measures are normally necessary for sub–stations of lower voltages.

– It is not permissible to withdraw or insert individual modules under voltage. In the withdrawn condition, some components are electrostatically endangered; during handling the standards for electrostatically endangered components must be observed. The modules are not endangered when plugged in.

WARNING! The relay is not designed for use in residential, commercial or light–industrial environment as defined in EN 50081.

3.1.6 Design

Housing	7XP20; refer to Section 2.1
Dimensions	refer to Section 2.2

Weight	7VE511	7VE512
– in housing for surface mounting	approx. 8 kg	approx. 12 kg
– in housing for flush mounting	approx. 6 kg	approx. 10 kg

Degree of protection acc. to EN 60529	
– housing	IP 51 *)
– terminals	IP 21

*) IP30 for cubicle installation; the degree of protection required for the point of installation must be ensured by the cubicle.

3.2 Paralleling

Setting ranges/steps

Active time T_A	1 s to 3600 s	(steps 1 s)
Minimum operating voltage U_{MIN}	40 V to 130 V	(steps 1 V)
Maximum operating voltage U_{MAX}	40 V to 130 V	(steps 1 V)
Voltage difference ΔU (separate for overvoltage and undervoltage)	0.0 V to 30.0 V	(steps 0.1 V)
Matching factor U_2/U_1 (for different voltage transformer voltages)	0.900 to 1.100	(steps 0.001)
Frequency difference Δf (separate for oversynchronous and subsynchronous)	0.00 Hz to 1.01 Hz	(steps 0.01 Hz)
Frequency difference for synchronous switching	10 mHz to 40 mHz	(steps 1 mHz)
Angle window $\Delta\varphi$	2° to 10°	(steps 1°)
Circuit breaker closing time T_{CB}	30 ms to 600 ms	(steps 1 ms); ∞
Command duration T_{CMD}	0.1 s to 1.0 s	(steps 0.1 s)
For synchronous closing:		
– Angle difference $\Delta\varphi$	0° to 45°	(steps 1°)
– Synchronous time T_{SYN}	1 s to 60 s or ∞ (no synchronous closing)	(steps 1 s)

Tolerances

Voltage thresholds U_{MIN} and U_{MAX}	3 % of set value
Voltage difference ΔU	5 % of set value or 0.3 V (matching factor $U_2/U_1 = 1$) 5 % of set value or 0.7 V (matching factor $U_2/U_1 \neq 1$)
Frequency difference Δf	10 mHz
Angles for synchronous switching	1° for $\Delta\varphi \leq 30°$ 2° for $\Delta\varphi > 30°$
Angles for asynchronous switching	3° for $\Delta f \leq 0.5$ Hz 5° for $\Delta f > 0.5$ Hz
Timers of synchronization functions	1 % of set value, however 10 ms
Timer of active time	1 % of set value, however 60 ms

Influence variables

– Auxiliary voltage in range $0.8 \leq U_H/U_{HN} \leq 1.15$	$\leq$ 1%
– Temperature in range 0 °C $\leq \vartheta_{amb} \leq$ 40 °C	$\leq$ 0.5 %/10 K
– Frequency in operating range	$\leq$ 2 %

3.3 Frequency and voltage balancing (for 7VE512 only)

Setting ranges/steps

Frequency balancer:

Operating range for frequency balancing (f1 must lie within the operating range acc. 3.1.1)	35 Hz to 70 Hz (to 80 Hz for f_N = 60 Hz)
Frequency range off−control oversynchronous Δf_{OSmax}, Δf_{OSmin}	0.01 Hz to 1.00 Hz (steps 0.01 Hz)
Frequency range off−control subsynchronous Δf_{SSmax}, Δf_{SSmin}	0.01 Hz to 1.00 Hz (steps 0.01 Hz)
Control duration factor over/subsynchronous K_C	1 to 10 (steps 1), refer to diagram Section 6.3.7, and 11 (continuous status indication)
min. control duration	30 ms to 300 ms (steps 1 ms)
Pause duration factor over/subsynchronous K_P	1 to 10 (steps 1), refer to diagram Section 6.3.7

Voltage balancer:

Operating range for voltage balancing	30 V to 130 V in frequency range 35 Hz to 70 Hz (to 80 Hz for f_N = 60 Hz) U1 must lie within the parameterized limit (Section 3.2)
Control duration factor over/undervoltage	1 to 10 (steps 1), refer to diagram Section 6.3.8, and 11 (continuous status indication)
min. control duration	30 ms to 300 ms (steps 1 ms)
Pause duration factor over/undervoltage	1 to 10 (steps 1), refer to diagram Section 6.3.8

Tolerances

Off−control ranges	10 mHz
Times	10 % of expected value $\pm$ 50 ms

Influence variables

– Auxiliary voltage in range $0.8 \leq U_H/U_{HN} \leq 1.15$	$\leq$ 1%
– Temperature in range $0\ °C \leq \vartheta_{amb} \leq 40\ °C$	$\leq$ 0.5 %/10 K

3.4 Ancillary functions

Operational value measurements

– Operational voltages phase–to–phase	$U1_{L1-L2}$; $U2_{L1-L2}$
Measurement range	0 V to 140 V
Tolerance	3 % of rated value
– Frequencies	f1, f2
Measurement range	40 Hz to 70 Hz
Tolerance	0.5 % of rated value
– Voltage magnitude difference	$\Delta U = \lvert U2 \rvert - \lvert U1 \rvert$
Measurement range	0 V to 140 V
Tolerance	2 % of rated value
– Frequency difference	$\Delta f = f2 - f1$
Measurement range	0 Hz to 30 Hz
Tolerance	10 mHz in operating range 0.5 % of rated value
– Angle difference	$\Delta\varphi = \varphi 2 - \varphi 1$
Measurement range	−180° to +180°
Tolerance	1°
– Phase sequence indication	U1 clockwise, counter–clock, wrong, without U2 clockwise, counter–clock, wrong, without
– selected setting parameter block	Block 1 or block 2 with 7VE511 Block 1 to block 6 with 7VE512

4 Method of operation

4.1 Operation of complete unit

The numerical paralleling device 7VE51 is equipped with a powerful and proven 16−bit microprocessor. This provides fully digital processing of all functions from data acquisition of measured values to the close signals for the circuit breakers.

Figure 4.1 shows the basic structure of the unit.

The measured value input section transforms the voltages from the measurement transformers and matches them to the internal processing level of the

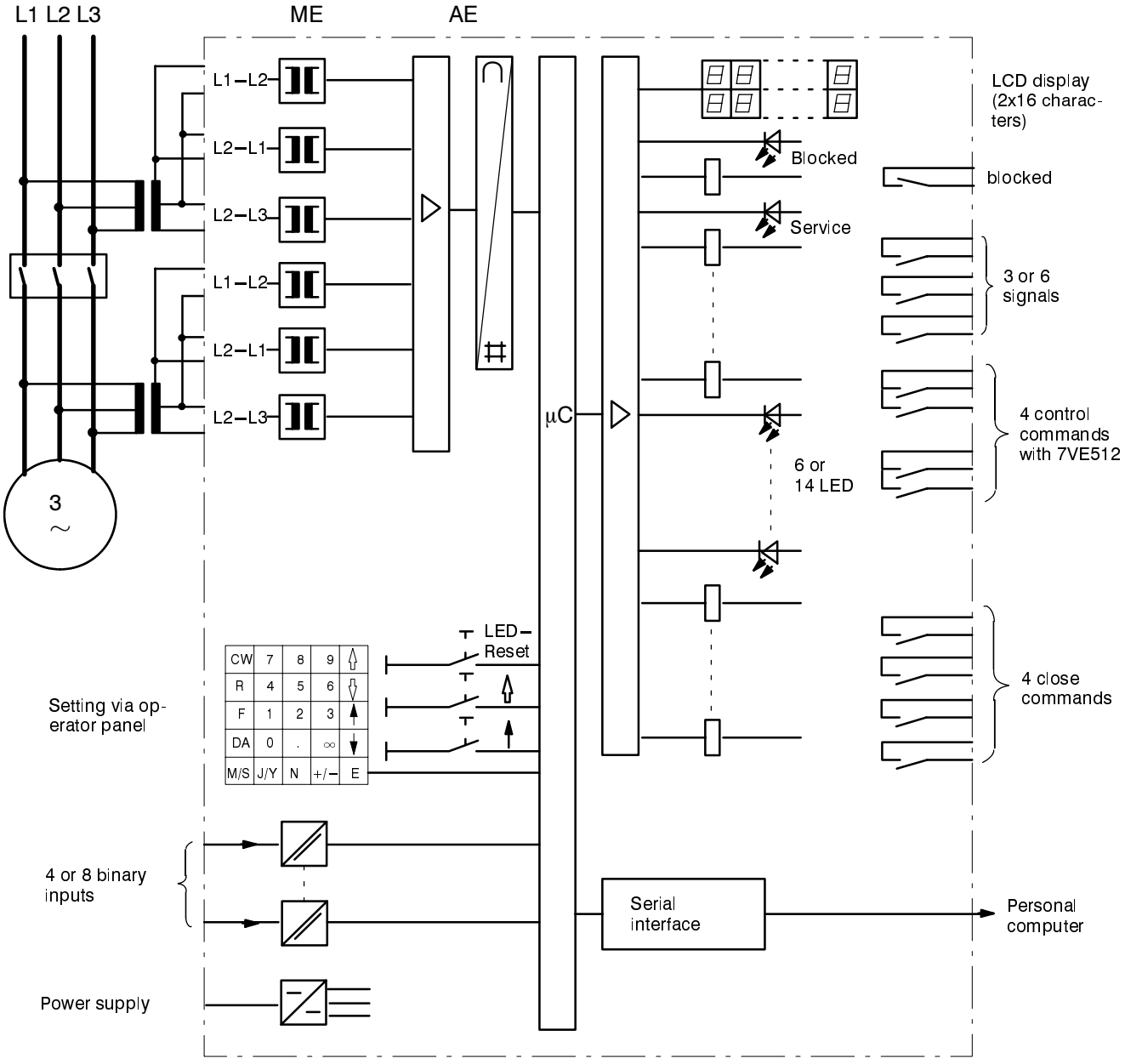


Figure 4.1 Hardware structure of paralleling device, example

unit. Apart from the galvanic and low−capacitive isolation provided by the input transformers, filters are provided for the suppression of interference. The filters have been optimized with regard to bandwidth and processing speed to suit the measured value processing. The matched analog values are then passed to the analog input on the processor p.c.b.

The analog input section contains input amplifiers, sample and hold elements for each input, analog−to−digital converters and memory circuits for the data transfer to the microprocessor.

For each measured voltage of the two sources (defined as U1 and U2), three measured value inputs are available. Two measured value inputs of each set will be connected to the (phase−to−phase) voltages which are to be paralleled, with respectively reversed polarity. In conjunction with the the two different and logically independent measuring methods and the two independently controlled closing relays, dual channel processing is achieved. The respective third measured value input can be used to connect another phase−to−phase voltage so that the unit is even able to check the phase sequence.

Apart from control and supervision of the measured values, the microprocessor processes the actual paralleling functions. These include in particular:

- filtering and formation of the measured quantities,
- calculation of the voltages and the voltage magnitude difference,
- calculation of the frequencies and the frequency difference,
- calculation of the phase angle difference,
- scanning of limit values and time sequences for synchronous switching,
- predetermination of the ideal closing instant for asynchronous switching,
- output of control commands to the voltage and speed regulator for automatic synchronization (in 7VE512),
- output of the closing command taking into account the breaker operating time,
- storage and issue of messages.

Binary inputs and outputs to and from the processor are channelled via the input/output elements. From these the processor receives information from the switchgear (e.g. start−to−synchronize) or from other equipment. Outputs include, in particular, the command to the circuit breaker, the control commands for voltage and speed (with 7VE512) and signals for remote signalling of important events and conditions as well as visual indicators (LEDs) and an alphanumerical display on the front plate.

Two command relays are provided for the closing command. These are dual channel controlled by each of the results of the two measurement methods. The contacts are connected in series so that a closing command can only be given when both relays have picked up.

An integrated membrane keyboard in connection with the built−in alphanumerical LCD display enables communication with the unit. All operational data such as setting values, plant data, etc. are entered into the device from this panel (refer to Section 6.3). Using this panel the parameters can be recalled and the relevant annunciations and messages can be read out (refer to Section 6.4). The dialog with the relay can be carried out alternatively via the serial interface in the front plate by means of a personal computer.

A power supply unit provides the auxiliary supply on the various voltage levels to the described functional units. +24 V is used for the relay outputs. The analog input requires ±15 V whereas the processor and its immediate peripherals are supplied with +5 V. Transient failures in the supply voltage, up to 50 ms, which may occur during short−circuits in the d.c. supply system of the plant are bridged by a d.c. voltage storage element (rated auxiliary voltage $\geq$ 110 Vdc).

4.2 Paralleling of generators with systems

For paralleling generators with networks, the device checks the network and generator voltages. Both voltage magnitudes must lie within the voltage operating limits; both frequencies must lie within the frequency operating limits. Following starting the relay checks the voltage magnitudes to see whether the set voltage difference ΔU is fallen below.

When the conditions are fulfilled, the device calculates the closing instant from the actual frequency difference and the set breaker operating time and then outputs the close command such that the voltage phasors of the network and generator voltages agree at the instant when the breaker poles touch each other.

4.3 Automatic synchronizing of generators

Fully automatic synchronizing of the generator with the network is possible in the model with frequency and voltage balancing (7VE512) provided the voltage magnitudes and frequencies lie within the operating range. The frequency balancer outputs control commands to the speed regulator of the driving machine and thus adjusts the generator frequency to the paralleling instant optimally and in a short time. At the same time, the generator voltage is matched to the network voltage by means of control commands to the voltage regulator. When setting the device it is possible to define whether paralleling is to take place only in the oversynchronous state, only in the subsynchronous state, or in both states of the machine.

The device calculates the command instant from the measured voltages as in 4.2.

4.4 Paralleling of systems

Paralleling of networks which are already synchronous via other connections depends on the condition that the difference in phase angle between the measured voltages does not exceed a set value for the duration of an adjustable time. The close command is output if the frequency and voltage differences are also within the set limits.

Asynchronous networks can also be paralleled. The device then determines the command instant as in 4.2.

It is possible to set individually for each paralleling location whether only asynchronous switching, only synchronous switching or both are to be permissible.

4.5 Output of status signals

7VE512 can be set to deliver status signal such like ”frequency too high” or ”too low”, ”voltage too high” or ”too low”, and ”phase angle positive” or ”negative”. These signals are then output instead of the balancing control signals. They may be processed by external devices or used as status check informations.

It can be selected whether the closing command should be issued only for synchronous paralleling (within settable limits of voltage magnitude difference, frequency difference and phase angle difference), or only for asynchronous paralleling (within settable limits of voltage magnitude difference and frequency difference and under consideration of the closing instant as explained in Section 4.2), or for both cases.

4.6 Measurement sequence

The sequence for processing the measured quantities is shown simplified in Figure 4.2.

The indices for the voltages are used as follows: the index 1 which is not a subscript identifies the fixed (non−regulated) voltage, index 2 the regulated voltage of the generator. Frequency and voltage balancing must therefore always have an effect on voltage U2. The assignment of these indices is irrelevant when paralleling networks. The indices as subscripts identify the phases, e.g. $U2_{L12}$ is the phase−to−phase voltage between phases L1 and L2 of the regulated side U2.

The measured voltages $U1_{L12}$, $\overline{U1_{L12}}$, $U1_{L23}$ and the measured voltages $U2_{L12}$, $\overline{U2_{L12}}$, $U2_{L23}$ are continuously entered as numerical values into a circulating buffer. Thus each of the six measured quantities has a corresponding sequence of numerical sample values in the circulating buffers. These sample values represent the variation of the analog variable with respect to time.

$\overline{U1_{L12}}$ is the voltage $U1_{L12}$ displaced by 180° and connected via a separate measured value input via separate sample and hold elements and separate analog−to−digital converter ranges. The same applies to $\overline{U2_{L12}}$ and $U2_{L12}$.

The voltages $U1_{L23}$ and $U2_{L23}$ are used in the device for the phase sequence check. Since they are of no significance when determining the paralleling conditions, they can be omitted.

The voltages displaced by 180° with respect to one another must always add up to zero. This enables constant monitoring of the measuring circuits, i.e. the sequence from the voltage transformer circuits up to the measured value memories.

The continuity of the measured quantities is also checked. The difference between two successive sample values of each measured voltage is checked to see whether it falls below a permissible value, since voltage jumps would influence determination of frequencies and phase angles.

To ensure that harmonics do not influence the results − which could lead to an operation failure − the voltages decisive for paralleling are filtered numerically and each stored in further filter buffers.

The measured voltages are now evaluated by means of two different methods. Each method operates with its own sets of measured values.

The magnitudes of the voltages are first examined and compared with the parameterized minimum and maximum values.

The first method operates according to the envelope curve principle. The instantaneous values of the envelope curve are determined from the beat function of the voltage difference. The time at which the envelope curve reaches a value of zero is calculated. A logical close command is generated taking into account the parameterized breaker operating time.

The second method operates according to the zero crossing principle. The difference in angle is determined from the zero crossings of the measured voltages. The synchronizing instant is calculated from the change in the zero crossings and a logical close command generated taking into account the parameterized breaker operating time.

The two methods of measurement are based on autonomous firmware blocks and make decisions independent of one another via the respective close command. Since the zero crossing method enables a higher accuracy with respect to the switching angle, an angle window is opened a few degrees earlier for the envelope curve method so that the accuracy of the close angle is determined by the zero crossing method without having to relinquish the high reliability of the envelope curve method.

The logical close commands of the two methods are each applied to different ports. These control the two coil poles of the close relay in a crosswise manner.

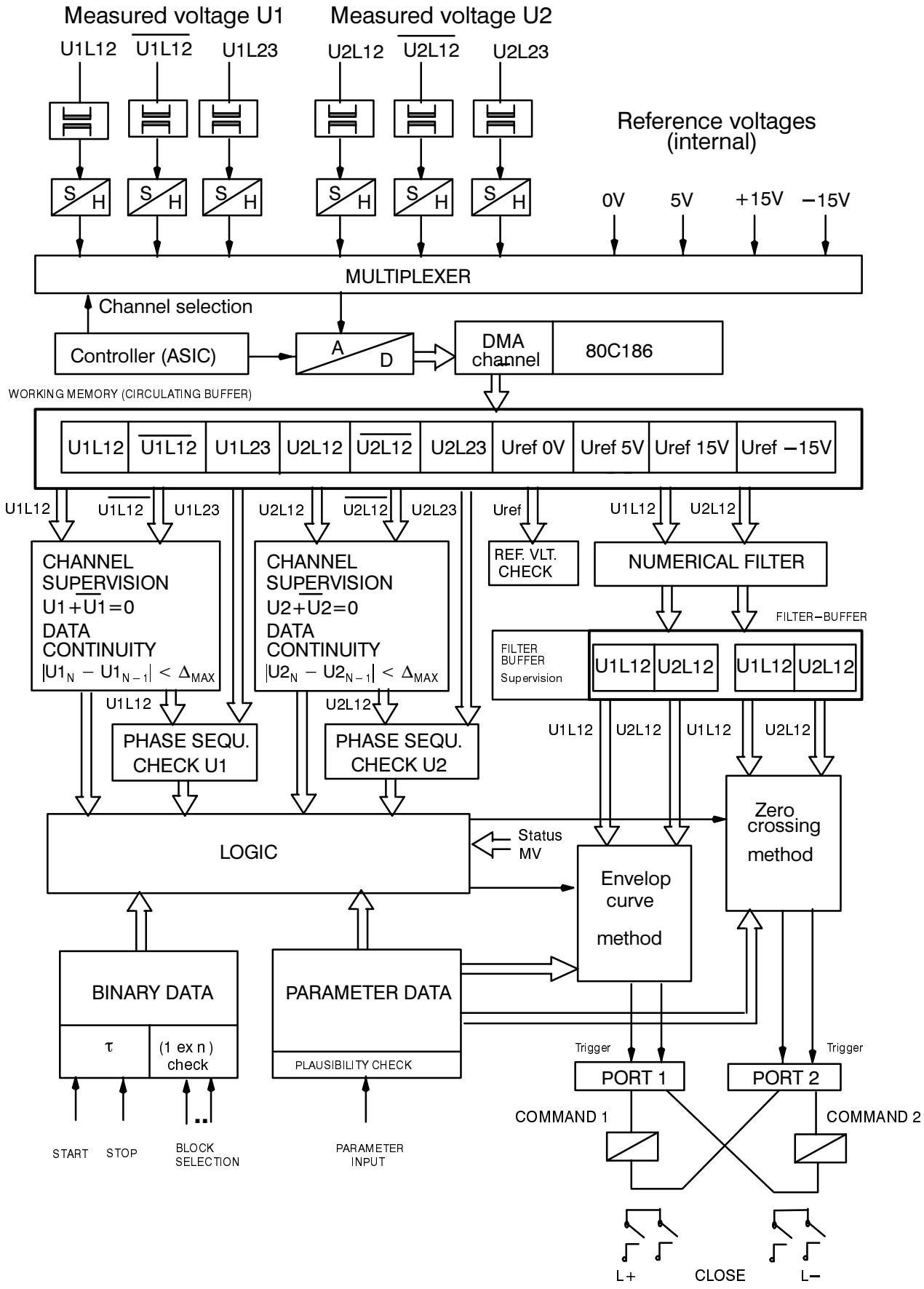


Figure 4.2 Dual channel design and processing in 7VE51

4.7 Ancillary functions

The ancillary functions of the paralleling device 7VE51 include:

– processing of annunciations,

– operational measurements,

– monitoring functions.

4.7.1 Processing of annunciations

4.7.1.1 Indications and binary outputs (signal relays)

Important events and conditions are indicated by optical indicators (LED) on the front plate. The unit also contains signal relays for remote indication.

The LED indicators can be tested by pressing the RESET LED button on the front, without opening the cover.

A green LED indicates readiness for operation. This LED remains illuminated when the microprocessor is working correctly and the unit is not faulty. The LED extinguishes when the self–checking function of the microprocessor detects a fault or when the auxiliary voltage is absent.

With the auxiliary voltage present but with an existing internal fault in the unit, a red LED illuminates (”Blocked”) and blocks the unit.

4.7.1.2 Information on the display panel or to a personal computer

A personal computer can be connected to the front interface of the numerical paralleling device. After synchronization, for example, important information concerning the history, such as start and close command, can be called up on the display of the device or via the front interface. The events are tagged with a relative time.

The events can also be read out with a personal computer. This provides the comfort of a CRT screen and menu–guided operation. Additionally, the data can be documented on a printer or stored on a floppy disc for evaluation elsewhere.

The device stores the data of the last three paralleling procedures; with a fourth paralleling the oldest event is overwritten in the memory.

4.7.2 Routine operational measurements

The r.m.s. values of the measured voltages are constantly available for recall locally or for remote data transfer. Furthermore, the voltages, the frequencies, the voltage and frequency differences, phase angles and phase sequences (if measured), as well as the selected parameter block, can be read off from the display or via the operating interface.

4.7.3 Monitoring functions

Numerical paralleling device 7VE51 incorporates comprehensive monitoring functions which cover both hardware and software.

4.7.3.1 Hardware monitoring

The unit is supervised from the measurement inputs to the command relays. Details are as follows:

– Measured quantities

  The measured voltages which are relevant for paralleling are twice fed to the device, with reversed polarity. Within the device they are transformed in two different channels, are led via two different sample–and–hold elements, two different analog/digital converters to two different buffer regions; they are continuously checked for plausibility and continuity. Discrepancies cause blocking of the device and an alarm. If the voltages are separated right from the voltage transformers, the voltage conductors are included in this supervision.

  If two phase–to–phase voltages are connected, the device checks the phase rotation, too. Faults cause blocking of the unit and an alarm.

– Auxiliary and reference voltages

  The processor monitors the auxiliary voltages for the multiplexer and offset and reference voltages for the ADC (Analog/Digital Converter). The device is blocked as soon as impermissible deviations occur; permanent faults are annunciated.

  Failure or switch–off the auxiliary voltage automatically puts the system out of operation; this status is indicated by a fail–safe contact. Transient dips in supply voltage of less than 50 ms will not disturb the function of the device.

– Trip circuits:

  The command relays are controlled by two command channels and one additional release channel. Discontinuities and short–circuits in the relay control circuits are monitored.

– Memory modules:

  A cyclic checksum is formed for the program memory (EPROM), the parameter assignment memory (EEPROM) and the working memory (RAM) and compared with the stored checksum. (The checksum of EEPROMs is calculated during each new parameter assignment process.)

4.7.3.2 Software monitoring

For continuous monitoring of the program sequences, a watchdog timer is provided which will reset the processor in the event of processor failure or if a program falls out of step. Further internal plausibility checks ensure that any fault in processing of the programs, caused by interference, will be recognized. Such faults lead to reset and restart of the processor.

If such a fault is not eliminated by restarting, further restarts are initiated. If the fault is still present after three restart attempts the system will switch itself out of service and indicate this condition by drop–off the availability relay, thus indicating ”equipment fault” and simultaneously the LED ”Blocked” comes on.

The dual channel processing of the measured values according two different measuring methods in conjunction with autonomous firmware modules as described in Section 4.6 meet the extreme safety requirement. The logical closing command of each channel is annunciated and logged.

5 Installation instructions

Warning

The successful and safe operation of this device is dependent on proper handling and installation by qualified personnel under observance of all warnings and hints contained in this manual.

In particular the general erection and safety regulations (e.g. IEC, DIN, VDE, or national standards) regarding the correct use of hoisting gear must be observed. Non−observance can result in death, personal injury or substantial property damage.

5.1 Unpacking and repacking

When dispatched from the factory, the equipment is packed in accordance with the guidelines laid down in IEC 255−21, which specifies the impact resistance of packaging.

This packing shall be removed with care, without force and without the use of inappropriate tools. The equipment should be visually checked to ensure that there are no external traces of damage.

The transport packing can be re−used for further transport when applied in the same way. The storage packing of the individual relays is not suited to transport. If alternative packing is used, this must also provide the same degree of protection against mechanical shock, as laid down in IEC 255−21−1 class 2 and IEC 255−21−2 class 1.

Before initial energization with supply voltage, the relay shall be situated in the operating area for at least two hours in order to ensure temperature equalization and to avoid humidity influences and condensation.

5.2 Preparations

The operating conditions must accord with VDE 0100/5.73 and VDE 0105 part 1/7.83, or corresponding national standards for electrical power installations.

Caution!

The modules of digital relays contain CMOS circuits. These shall not be withdrawn or inserted under live conditions! The modules must be so handled that any possibility of damage due to static electrical charges is excluded. During any necessary handling of individual modules the recommendations relating to the handling of **e**lectrostatically **e**ndangered **c**omponents (EEC) must be observed.

In installed conditions, the modules are in no danger.

5.2.1 Mounting and connections

5.2.1.1 Model 7VE51⋆⋆–⋆D⋆⋆⋆ for panel surface mounting

– Secure the unit with four screws to the panel. For dimensions refer to Figure 2.2 or 2.4.

– Connect earthing terminal (Terminal 16 or 26) of the unit to the protective earth of the panel.

– Make a solid low–ohmic and low–inductive operational earth connection between the earthing surface at the side of the unit using at least one standard screw M4, and the earthing continuity system of the panel; recommended grounding strap DIN 72333 form A, e.g. Order–No. 15284 of Messrs Druseidt, Remscheid, Germany.

– Make connections via screwed terminals.

5.2.1.2 Model 7VE51⋆⋆–⋆C⋆⋆⋆ for panel flush mounting or –⋆E⋆⋆⋆ for cubicle installation

– Lift up both labelling strips on the lid of the unit and remove cover to gain access to four holes for the fixing screws.

– Insert the unit into the panel cut–out and secure it with the fixing screws. For dimensions refer to Figure 2.3 or 2.5.

– Connect earthing screw on the rear of the unit to the protective earth of the panel or cubicle.

– Make a solid low–ohmic and low–inductive operational earth connection between the earthing surface at the rear of the unit using at least one standard screw M4, and the earthing continuity system of the panel or cubicle; recommended grounding strap DIN 72333 form A, e.g. Order–No. 15284 of Messrs Druseidt, Remscheid, Germany.

– Make connections via the screwed or snap–in terminals of the sockets of the housing. Observe labelling of the individual connector modules to ensure correct location; observe the max. permissible conductor cross–sections. The use of the screwed terminals is recommended; snap–in connection requires special tools and must not be used for field wiring unless proper strain relief and the permissible bending radius are observed.

5.2.2 Checking the rated data

The rated data of the unit must be checked against the plant data. This applies in particular to the auxiliary voltage.

5.2.2.1 Control d.c. voltage of binary inputs

When delivered from factory, the binary inputs are designed to operate in the total control voltage range from 19 V to 288 V. If the rated control voltage for binary inputs is 110 V or higher, it is advisable to fit a higher pick–up threshold to these inputs to increase stability against stray voltages in the d.c. circuits.

To fit a higher pick–up threshold of approximately 80 V to a binary input a solder bridge must be removed. Figure 5.1 shows the assignment of these solder bridges for the inputs BI 1 to BI 4, and their location on the basic p.c.b. of the basic input/output module GEA. Figure 5.2 shows the assignment of these solder bridges for the inputs BI 5 to BI 8 and their location on the additional input/output module ZEA (only available with 7VE512).

– Open housing cover.

– Loosen the basic module using the pulling aids provided at the top and bottom.

Caution!

Electrostatic discharges via the component connections, the PCB tracks or the connecting pins of the modules must be avoided under all circumstances by previously touching an earthed metal surface.

– Pull out basic module and place onto a conductive surface.

– Check the solder bridges according to Figure 5.1, remove bridges where necessary.

– Insert basic module into the housing; ensure that the releasing lever is pushed fully to the left before the module is pressed in.

– Firmly push in the module using the releasing lever.

– Similarly check solder bridges on additional input/output module according to Figure 5.2. This smaller module has pulling handles instead of the releasing lever (only 7VE512).

– Close housing cover.

The assignment of the binary inputs and their meaning is shown in Table 5.1.

Binary input	Meaning	Module	Bridge
1	Start	GEA	X21
2	Parameter set 1	GEA	X22
3	Parameter set 2	GEA	X23
4	Stop	GEA	X24
5 *)	Parameter set 6	ZEA	X7
6 *)	Parameter set 3	ZEA	X8
7 *)	Parameter set 4	ZEA	X9
8 *)	Parameter set 5	ZEA	X10

*) only 7VE512

Table 5.1 Assignment of the binary inputs

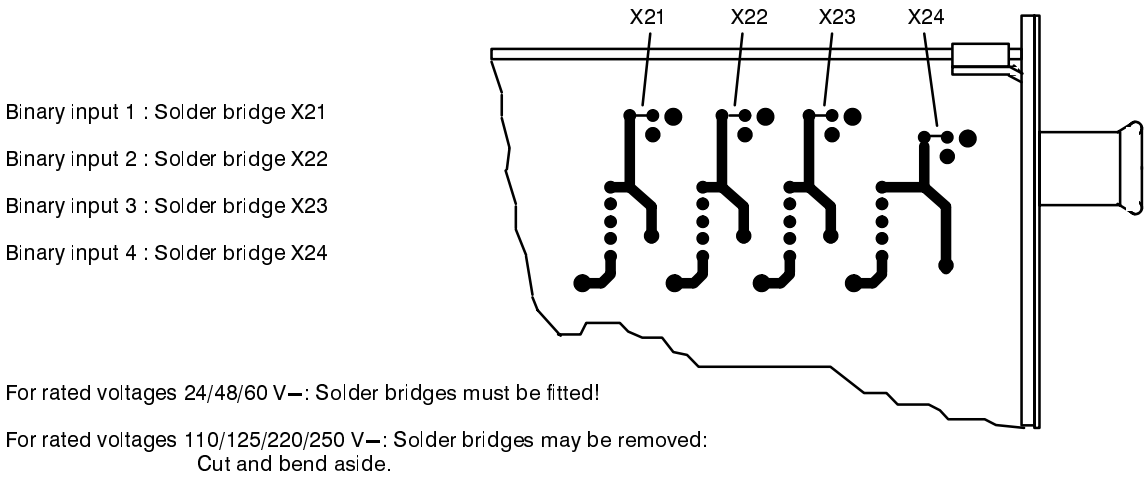


Figure 5.1 Checking for control voltages for binary inputs 1 to 4 on basic module GEA

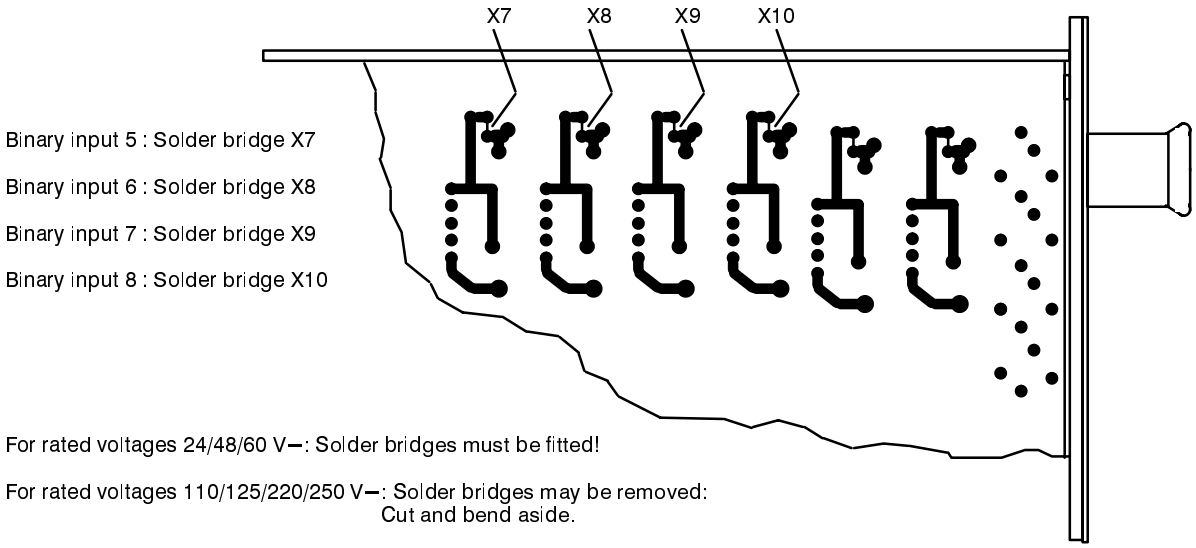


Figure 5.2 Checking for control voltages for binary inputs 5 to 8 on additional module ZEA (only 7VE512)

5.2.3 Connections

General and connection diagrams are shown in Appendix A and B. For paralleling, one phase–to–phase voltage U_{L1-L2} of each side of the breaker must be connected. A further phase–to–phase voltage U_{L2-L3} should be connected if available. Thus, the device will be able to check the phase sequence of the voltages. The voltages may be derived from three star connected voltage transformers (U_{L1-N}, U_{L2-N}, U_{L3-N}) or from two phase–to–phase connected voltage transformers (U_{L1-L2}, U_{L2-L3}, so called V–connection).

Connection to two phase–to–phase voltages must be carried out at both sides of the breaker if used at all. In this case phase sequence check must be set effective both sides (Section 6.3.5, addresses 2*03 and 2*04). Different connection for the both sides is not permitted!

Phase rotation must be equal at both sides of the breaker, both clockwise or both counter–clockwise. If they are different, two phases must be interchanged at one side, already in the primary plant. It must be ensured that at all three breaker poles equal voltages are present when the systems (or system and generator) are in synchronism. Equal phase rotations must be present on the circuit breaker as well as at the device

If synchronizing should be performed via a unit block transformer, the voltages must be adapted in accordance with the vector group of the block transformer. Connection examples with intermediate voltage transformers are shown in appendix B.

It is imperative that the voltages have equal phase at the breaker poles when they have equal phase at the terminals of the device, according connection diagrams in appendix B.

The voltage transformer secondary leads must be installed in such a way that the conductors of one voltage transformer set are laid together, particularly if the device is connected to different paralleling locations (switch–over of the voltages). They must once be earthed at the voltage transformers. This is to avoid interferences by inductive or capacitive influences. Stranded and screened cables are recommended. This is in order to ensure that, particularly in extended substation, equal longitudinal voltages could be induced into the leads but practically no transverse voltage will occur.

Furthermore, the voltage transformer cables must be screened in order to ensure proper electro–magnetic compatibility, and the screens must be earthed at both sides.

Similarly, the control commands between the device and various selected locations must be installed such that at last equal longitudinal voltages should be induced into two respective cores of a conductor loop: Each control cable must incorporate at least one return conductor; the remaining control cores should be arranged symmetrically around this return conductor. Conductors not use should be earthed at both ends to increase screening effect.

5.2.4 Checking the connections

Warning

Some of the following test steps are carried out in presence of hazardous voltages. They shall be performed by qualified personnel only which is thoroughly familiar with all safety regulations and precautionary measures and pay due attention to them.
Non−observance can result in severe personal injury.

Before initial energization with supply voltage, the relay shall be situated in the operating area for at least two hours in order to ensure temperature equalization and to avoid humidity influences and condensation.

– Switch off the circuit breakers for the d.c. supply and the voltage transformer circuits!

– Check the continuity of all the voltage transformer circuits against the plant and connection diagrams:

  - Are the voltage transformers correctly earthed?
  - Are the polarities of the voltage transformer circuits correct?
  - Is the assignment of the voltage transformers correct (voltages U1, U2)?
  - Is the assignment of the control commands (decrease/increase frequency or voltage) correct (applicable for 7VE512 only)?

  Attention! If more than one synchronizing location is used, it is most important to check that the assignment of measured voltages, closing command, parameter block selection and, if applicable, the control commands for each selectable location is correct!

– Ensure that the miniature slide switch on the front plate is in the "OFF" ◯· position. (refer Figure 6.1 or 6.2).

– Fit a d.c. ammeter in the auxiliary power circuit; range approx. 1.5 A to 3 A.

– Close the battery supply circuit breaker; check polarity and magnitude of voltage at the terminals of the unit or at the connector module.

– The measured current consumption should be insignificant. Transient movement of the ammeter pointer only indicates the charging current of the storage capacitors.

– Put the miniature slide switch of the front plate in the "ON" position ⊙ . The unit starts up and, on completion of the run−up period, the green LED on the front comes on, the red LED gets off after at last 5 sec.

– Open the circuit breaker for the d.c. power supply.

– Remove d.c. ammeter; reconnect the auxiliary voltage leads.

– Check through the closing circuits to the circuit breaker(s). Ensure that the contacts of the two close relays are connected in series.

– Check through the control wiring to and from other devices.

Warning for 7VE512

If the model 7VE512 is used for several selectable synchronizing locations and the control commands should be given before the start−to−parallel signal (refer to Section 6.3.7, address 2*17 for frequency balancer; Section 6.3.8, address 2*26 for the voltage balancer), it must be ensured that the device is not switched to its supply voltage before the measured voltages and control leads are switched to the respective location! This is to ensure that the control commands are always given to the correct synchronizing location.

It is reasonable that connection of the supply voltage is coupled with the selection of the location on the selector switch.

If only one synchronizing location is used, connection of the measured voltages and the control command can be fixed.

– Check the signal circuits.

– Reclose the protective m.c.b.'s.

6 Operating instructions

6.1 Safety precautions

Warning

All safety precautions which apply for work in electrical installations are to be observed during tests and commissioning.

Caution!

Connection of the device to a battery charger without connected battery may cause impermissibly high voltages which damage the device. See also Section 3.1.1 under Technical data for limits.

6.2 Dialog with the device

Setting, operation and interrogation of digital protection and automation systems can be carried out via the integrated membrane keyboard and display panel located on the front plate. All the necessary operating parameters can be entered and all the information can be read out from here. Operation is, additionally, possible via the interface socket by means of an operator terminal or personal computer.

6.2.1 Membrane keyboard and display panel

The membrane keyboard and display panel is externally arranged similar to a pocket calculator. Figure 6.1 or figure 6.2 illustrates the front view.

A two−line, each 16 character, liquid crystal display presents the information. Each character comprises a 5 x 8 dot matrix. Numbers, letters and a series of special symbols can be displayed.

During dialog, the upper line gives a four figure number, followed by a bar. This number presents the **setting address**. The first two digits indicate the address **block**, then follows the two−digit **sequence number**.

The keyboard comprises 28 keys with numbers, Yes/No and control buttons. The significance of the keys is explained in detail in the following.

Numerical keys for the input of numerals:

0 to 9		Digits 0 to 9 for numerical input
•		Decimal point
∞		Infinity symbol
+/−		Change of sign (input of negative numbers)

Yes/No keys for text parameters:

J/Y	YES key: operator affirms the displayed question
N	NO key: operator denies the displayed question or rejects a suggestion and requests for alternative

Keys for paging through the display:

↑	Paging forwards: the next address is displayed
↓	Paging backwards: the previous address is displayed
⇧	Block paging forwards: the beginning of the next address block is displayed
⇩	Block paging backwards: the beginning of previous address block is displayed

Confirmation key:

E	Enter or confirmation key: each numerical input or change via the YES/NO keys must be confirmed by the enter key; only then does the device accept the change. The enter key can also be used to acknowledge and clear a fault prompt in this display; a new input and repeated use of the enter key is then necessary.

Control and special keys:

CW	Codeword: prevents unauthorized access to setting programs (not necessary for call−up of annunciations or messages)
R	Backspace erasure of incorrect entries
F	Function key: not used
DA	Direct addressing: if the address number is known, this key allows direct call−up of the address
M/S	Messages/Signals: interrogation of annunciations of operating data (refer to Section 6.4)

The three keys ↑ ; ⇑ ; RESET which are somewhat separated from the rest of the keys, can be accessed when the front cover is closed. The arrows have the same function as the keys with identical symbols in the main field and enable paging in forward direction. Thus all setting values and event data can be displayed with the front cover closed. Furthermore, the LED indications on the front can be tested via the RESET key without opening the front cover.

6.2.2 Operation with a personal computer

A personal computer allows, just as the operator panel, all the appropriate settings, initiation and read−out of data, but with the added comfort of screen−based visualization and a menu−guided procedure.

All data can be read in from, or copied onto, magnetic data carrier (floppy disc) (e.g. for settings and configuration). Additionally, all the data can be documented on a connected printer.

For operation of the personal computer, the instruction manuals of this device are to be observed. Note that the operating interface in the front of the relay is not galvanically isolated and that only adequate connection cables are applied (e.g. 7XV5100−2). Further information about facilities and suitable down−loader programs on request.

6.2.3 Operational preconditions

For most operational functions, the input of a codeword is necessary. This applies for all entries via the membrane keyboard or front interface which concern the operation on the relay, for example

– setting of operational parameters (thresholds, functions).

The codeword is not required for the read−out of annunciations, operating data or messages, or for the read−out of setting parameters.

To indicate authorized operator use, press key **CW**, enter the six figure code 000000 and confirm with **E**. Codeword entry can also be made retrospectively, when an attempt to make an entry or to alter a parameter is responded to with the display ”NOT AUTHORIZED”.

```
CODEWORD  INPUT:
@ @ @ @ @ @
```

```
CW  ACCEPTED
```

The entered characters do not appear in the display, instead only a symbol @ appears. After confirmation of the correct input with **E** the display responds with **CW ACCEPTED**. Press the entry key **E** again.

```
CODEWORD  WRONG
```

If the codeword is not correct the display shows **CODEWORD WRONG**. Pressing the **CW** key allows another attempt at codeword entry.

If the codeword is accepted, parameterization can begin.

6.2.4 Representation of the 7VE51 (front views)

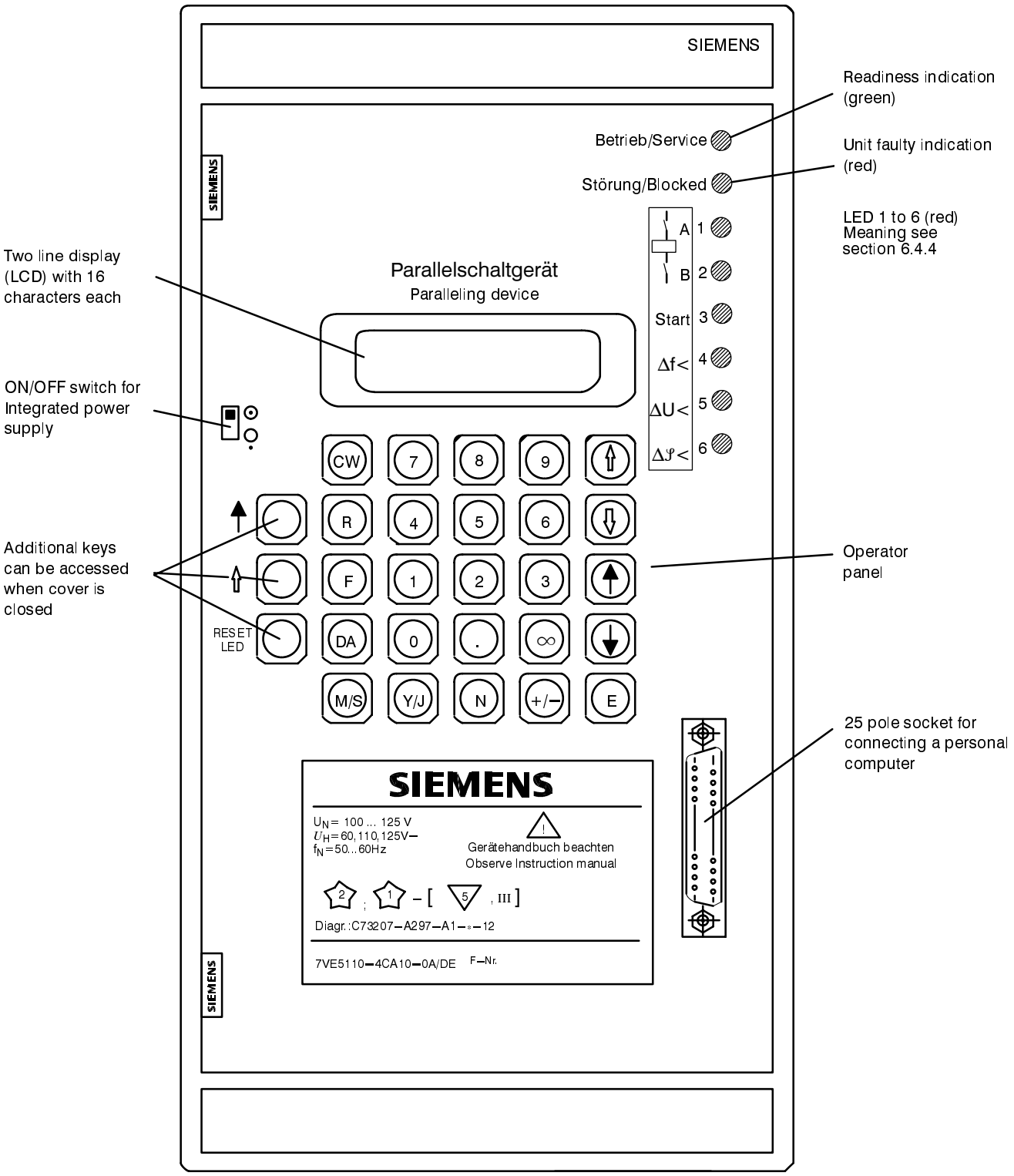


Figure 6.1 Front view 7VE511

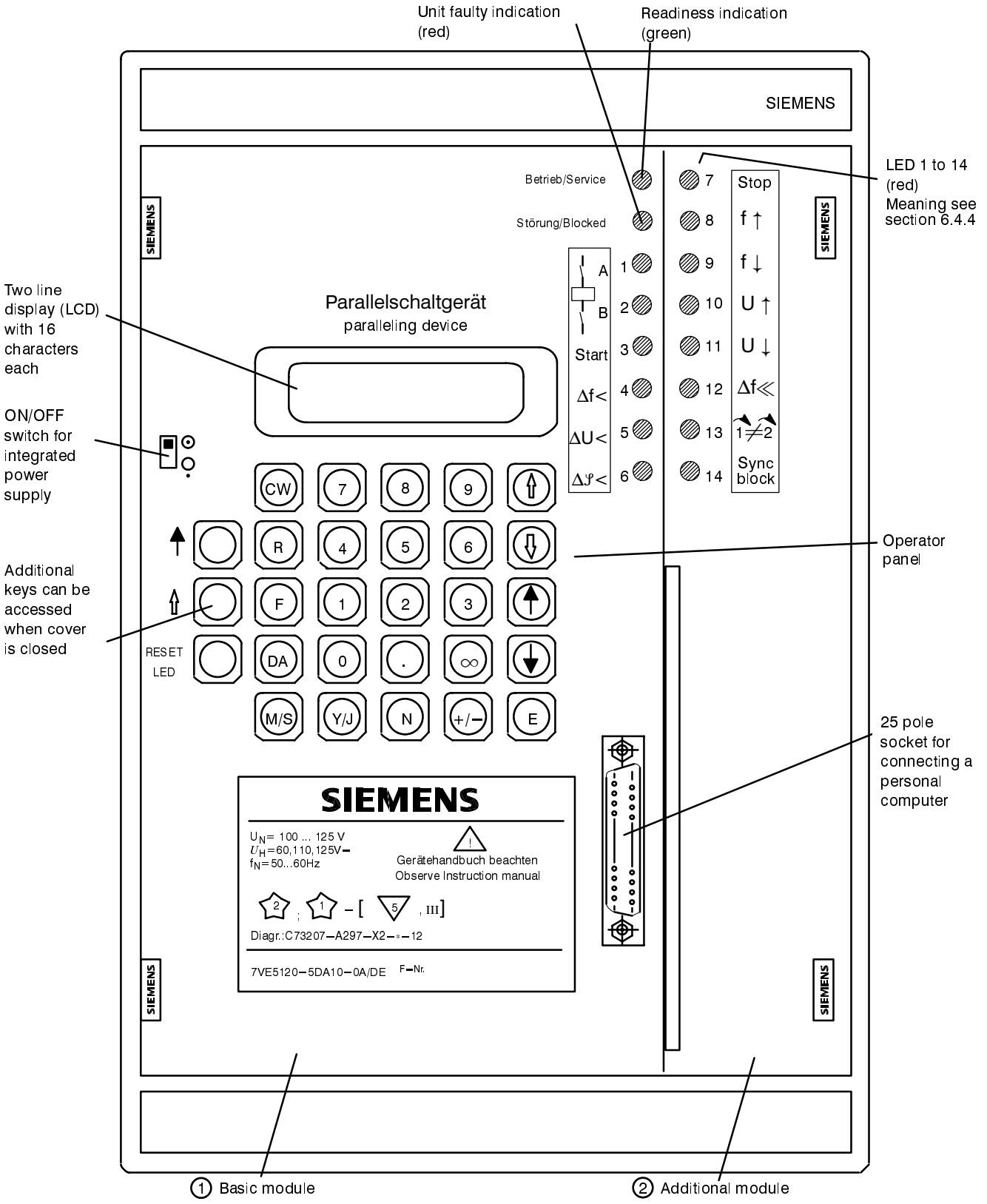


Figure 6.2 Front view 7VE512

6.3 Setting the operational parameters

6.3.1 Introduction

For setting the operational parameters it is necessary to enter the codeword (see 6.2.3). Without codeword entry, parameters can be read out but not be changed.

If the codeword is accepted, parameterizing can begin. In the following sections each address is illustrated in a box and is explained.There are three forms of display:

– Addresses without request for operator input

  The address is identified by the block number followed by 00 as sequence number (e.g. **11**00 for block **11**). Displayed text forms the heading of this block. No input is expected. By using keys ⇑ or ⇓ the next or the previous block can be selected. By using the keys ↑ or ↓ the first or last address within the block can be selected and paged.

– Addresses which require numerical input

  The display shows the four–digit address, i.e. block and sequence number (e.g. **2101** for block **21**, sequence number **1**). Behind the bar appears the meaning of the required parameter, in the second display line, the value of the parameter. When the device is delivered a value has been preset. In the following sections, this value is shown. If this value is to be retained, no other input is necessary. One can page forwards or backwards within the block or to the next (or previous) block. If the value needs to be altered, it can be overwritten using the numerical keys and, if required, the decimal point or, where appropriate, change sign (+/–) or infinity sign ∞. The permissible setting range is given in the following text, next to the associated box. Entered values beyond this range will be rejected. The setting steps correspond to the last decimal place as shown in the setting box. Inputs with more decimal places than permitted will be truncated down to the permissible number. **The value must be confirmed with the entry key E!** The display then confirms the accepted value. The values are finally and securely stored in the device only after completion of the parameter setting process (see below).

– Addresses which require text input

  The display shows the four–digit address, i.e. block and sequence number (e.g.**2104** for block **21**, sequence number **4**). Behind the bar appears the meaning of the required parameter, in the second display line, the applicable text. When the device is delivered, a text has been preset. In the following sections, this text is shown. If it is to be retained, no other input is necessary. One can page forwards or backwards within the block or to the next (or previous) block. If the text needs to be altered, press the "No"–key **N**. The next alternative text, also shown in the display boxes illustrated in the following sections, then appears. If the alternative text is not desired, the **N** key is pressed again, etc. The alternative which is chosen, **is confirmed with the entry key E.**

For each of the addresses, the possible parameters and text are given in the following sections. If the meaning of a parameter is not clear, it is usually best to leave it at the factory setting. The arrows ⇑ ⇓ or ↑ ↓ at the left hand side of the illustrated display boxes indicate the method of moving from block to block or within the block. Unused addresses are automatically passed over.

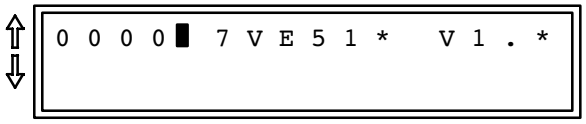
If the parameter address is known, then direct addressing is possible. This is achieved by depressing key **DA** followed by the four–digit address and subsequently pressing the enter key **E**. After direct addressing, paging by means of keys ⇑ ⇓ and keys ↑ ↓ is possible.

The parameterizing process can be ended at any time by depressing one of the keys ⇑ ⇓ which changes the parameter block. The displayed question "SETTINGS COMPLETED?" is then answered with the "Yes"–key **J**/**Y**. The question "SETTINGS COMPLETED?" appears each time a new block is chosen. If further parameters are to be changed, the question should be answered by pressing the "No"–key **N**.

After completion of the parameterizing process, the changed parameters which so far have only been stored in volatile memory, are then permanently stored in EEPROMs. The display confirms "SETTINGS EXECUTED".

6.3.2 Initial displays – address blocks 00 and 10

When the device has been switched on or the operator terminal has been connected, firstly the address 0000 and the type identification of the device appears. All Siemens products have an MLFB (machine readable type number).



The device introduces itself by giving its type number and the version of firmware with which it is equipped.

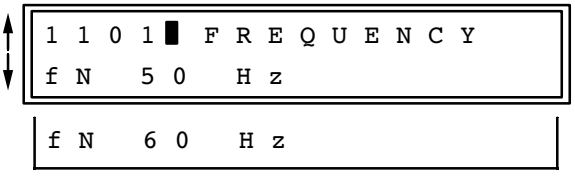
After adress 1000, the setting parameters begin. Further address possibilities are listed under ”Annunciations”.

Commencement of setting parameter blocks

6.3.3 Power system data – address block 11

The unit requires the input of some plant data.

Beginning of the block ”Power system data”



Rated system frequency
50 Hz or *60 Hz*

6.3.4. General information on parameter blocks

The setting parameters (functions, limits) for synchro–checks and paralleling are organized in address blocks. Each address block corresponds to a set of parameters which are decisive for the synchronization. Binary inputs can be used to select which block – and thus which functions and limits – are currently decisive. The parameter sets can thus be selected for the respective paralleling process from different synchronize locations.

The model **7VE511** provides **two** parameter sets of this type which are set in address blocks **21** and **22.**

The model **7VE512** provides **six** parameter sets of this type which are set in address blocks **23** to **28.**

The following paragraphs refer to the parameter sets of blocks 21 or 23 as representatives for all sets. The same consecutive address numbers apply analogously to the other blocks. The parameters 2318 to 2333 are only present in model 7VE512 with frequency and voltage balancing.

The following uniform **definition of the indices** for voltages, angles and frequencies applies to the parameters:

Index **1** for the constant reference variables (network, bus–bar),

Index **2** for the regulated variables (generator).

It is essential to observe this assignment in models with voltage and frequency balancing since the control commands must act on U2 and f2. The device has a completely symmetrical design with respect to the measured variables, apart from this essential definition, so that U1 and U2 can be selected optionally in networks.

6.3.5 Settings for function range

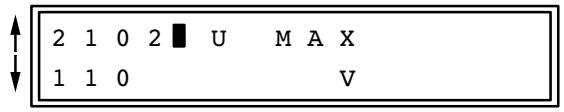
The operating range for the paralleling device is defined in addresses 2101 and 2102. A close command is not output if one of the voltages U1 or U2 drops below the set minimum voltage U MIN or rises above U MAX. The set value refers to the phase–to–phase measured voltages for paralleling $U1_{L1-L2}$ and $U2_{L1-L2}$.

One phase–to–phase voltage of each side $U1_{L1-L2}$ and $U2_{L1-L2}$ is sufficient in each case for paralleling.

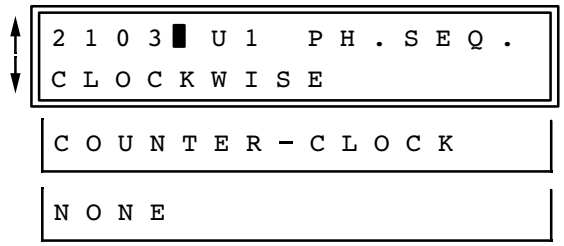
The device carries out a phase sequence check if the phase–to–phase voltages $U1_{L2-L3}$ and $U2_{L2-L3}$ are connected in addition (V–connection). The phases may be counter–clockwise or clockwise (addresses 2103 and 2104). The same phase rotation must be parameterized for both sides (U1 and U2). If the two phase–to–phase voltages are not connected for both sides, the parameters must both be set to *NONE*.

Beginning of the block ”Parameter set 1”,
first selectable parameter block

Minimum operation limit of measured voltages
for paralleling (phase–to–phase)
Setting range: **40** V to **130** V



Maximum operation limit of measured voltages
for paralleling (phase–to–phase)
Setting range: **40** V to **130** V

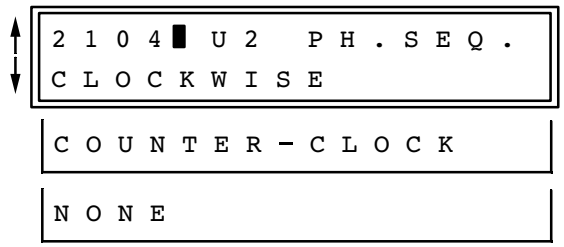


Phase sequence for check of voltage U1:

CLOCKWISE – U1 clockwise

COUNTER–CLOCK – U1 counter–clockwise

NONE – no phase sequence check



Phase sequence for check of voltage U2:

CLOCKWISE – U2 clockwise

COUNTER–CLOCK – U2 counter–clockwise

NONE – no phase sequence check

6.3.6 Settings for paralleling

For automatic paralleling, the permissible limits ΔU, Δf and Δφ must be set to check the synchronism.

The voltage difference ΔU can be set separately for U2 > U1 and U2 < U1 (addresses 2105 and 2106). Paralleling is not possible in the corresponding range with a setting of 0 V. It is not meaningful to set both voltage differences to 0 V since this condition cannot be satisfied in practice.

The frequency difference Δf can also be set separately for oversynchronous (f2 > f1) and subsynchronous (f2 < f1) switching (addresses 2107 and 2108). Paralleling is not possible in the corresponding range with a setting of 0 Hz; the frequency balancer controls into the other range in this case if frequency balancing can be carried out (7VE512). The circuit breaker closing time T_{CB} (address 2112) is decisive for the actual frequency difference limit in addition to the setting Δf: with high circuit breaker closing times, the permissible frequency difference is reduced as shown in Figure 6.3. **Only synchronous switching** is possible if both frequency limits are set to 0 Hz.

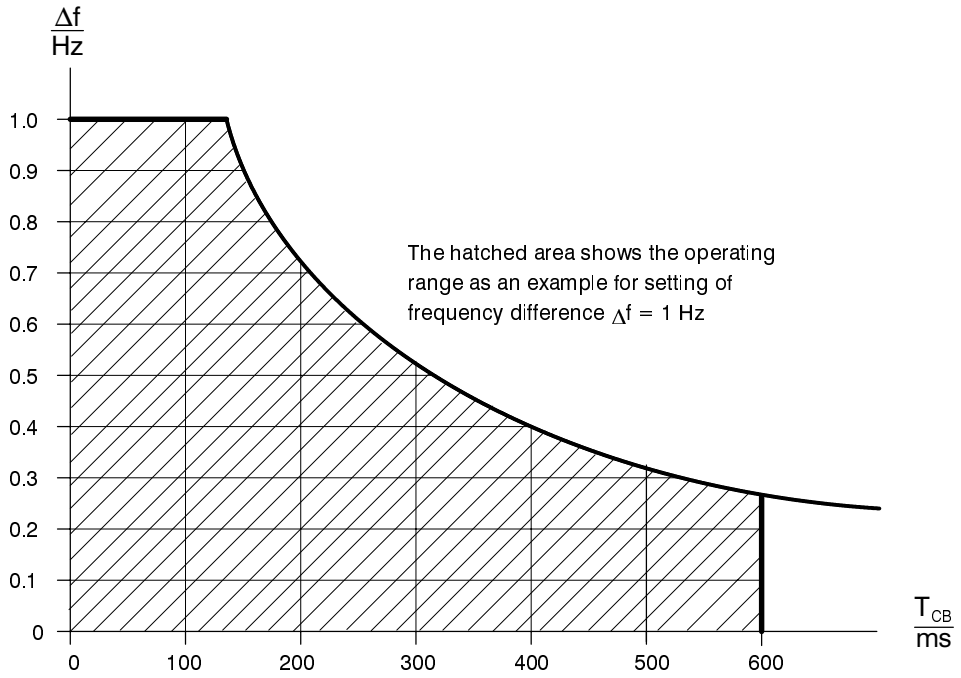


Figure 6.3 Maximum frequency difference Δf in dependence of the setting of circuit breaker closing time T_{CB} (parameter CB CLOSE TM, address 2112)

Permissible voltage difference ΔU if U2 greater than U1
Setting range: **0.0** V to **30.0** V;
With setting 0.0 V paralleling is not possible if U2 > U1

Permissible voltage difference ΔU if U2 smaller than U1
Setting range: **0.0** V to **30.0** V;
With setting 0.0 V paralleling is not possible if U2 < U1

Permissible frequency difference Δf if f2 greater than f1 (oversynchronous)
Setting range: **0.00** Hz to **1.01** Hz;
With setting 0.00 Hz paralleling is not possible if f2 > f1

Permissible frequency difference Δf if f2 smaller than f1 (subsynchronous)
Setting range: **0.00** Hz to **1.01** Hz;
With setting 0.00 Hz paralleling is not possible if f2 < f1

The parameters 2109 and 2110 are relevant to the switching of synchronous systems. The setting DELTA PHI (address 2109) defines the limits within which the difference in angle must lie. **Synchronous switching is not possible** with a setting of 0°.

The synchronous conditions must be satisfied for the duration T_{SYN} set under SYNCH.TIME (address 2110). When this time is set to ∞, synchronous switching is not possible.

Permissible angle difference Δφ for paralleling synchronous systems
Setting range: **0**° to **45**°
With setting 0° synchronous switching is blocked

Limit values ΔU, Δf and Δφ must not be exceeded during this time
Setting range: **1** s to **60** s
or ∞ (synchronous switching is blocked)

The parameters 2111 and 2112 are relevant to asynchronous switching. The parameter ANGLE WINDW (address 2111) defines by how many degrees the envelope curve method enables closing prior to the zero crossing method. The two−channel evaluation in model 7VE51 requires that the more exact zero crossing method defines the exact closing instant, and thus the envelope curve method must have enabled earlier than the zero crossing method.

Using the closing time of the circuit breaker T_{CB} (address 2112), the device determines the instant at which the command must be sent so that the synchronous moment is exactly reached when the breaker poles close. A meaningful breaker closing time is only in the hatched area of Figure 6.3. Closing does not take place if the breaker closing time is set to ∞ (factory setting); frequency and voltage balancing are, nevertheless, in operation, if present (7VE512).

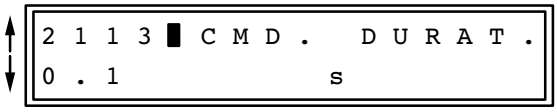
Angle window between command of envelope curve method and zero crossing method
Setting range: **2**° to **10**°

Closing time of the circuit breaker: Time between command output and closing instant of the breaker poles
Setting range: **30** ms to **600** ms or ∞;
with setting ∞ closing is blocked; voltage and frequency balancer operate, if available

---

Address 2113 is used to set the duration of the close command to the circuit breaker. This duration must always be greater than the closing time (address 2112); it must be sufficiently long such that it can be guaranteed that the circuit breaker has completely finished closing and has interrupted the close control circuit by means of its auxiliary contact.

The active time (address 2114) determines how long the device remains ready for measurements and operation following starting. The conditions for paralleling must be satisfied within this time. A close command no longer takes place after this time.



Duration of close command
Setting range: **0.1** s to **1.0** s

During the active time, the device is ready for measurement and operation
Setting range: **1** s to **3600** s
or ∞, i.e. device is operational until paralleling command is given or operation is stopped (via binary input)

Different secondary voltages U1 and U2 may be present at the voltage transformers even with equal primary voltages, due to different transformation ratios or other tolerances. Address 2117 allows to match to this difference. The Factor U2/U1 is the calculated or measured ratio of the secondary voltages; correction is made internally with the reference voltage U1, i.e. $U1_{processed} = U1_{measured} \bullet$ Factor.

Matching factor for secondary voltages
Setting range: **0.900** to **1.100**
Presetting is 1.000, i.e equal voltages, no correction

In order to ensure that the relay cannot be started again after successful synchronization at a certain synchronization location, the relay should be locked against further initiation with the same parameter set (address 2135). A renewed start with the same parameter set is then only possible after a stop signal is entered via a binary input.

During tests, or for special applications, it may be meaningful to switch this locking off. In this case, the relay does not check that the next start is carried out with a different parameter set. It is then not necessary to stop the relay after each synchronization attempt e.g. for dummy synchronizations during tests or commissioning.

Block starting with the actual parameter set after synchronization

ON – normal setting

OFF – during test, dummy synchronization, or similar

Address 2136 DELTA f SYN defines the limit within which the frequency difference must lie when the voltages are regarded as synchronous. Above this frequency difference, asynchronous closing is possible under consideration of the voltage magnitude difference, frequency difference and the circuit breaker closing time. Below this frequency difference, only synchronous switching is possible.

Permissible frequency difference for synchronous switching
Setting range: **10** mHz to **40** mHz

6.3.7 Settings for frequency balancing (7VE512 only)

Switching *ON*/*OFF* of the frequency balancer;

OFF – no frequency balancing

with *ON* a choice can be made:

after start – frequency balancing commences only after start command

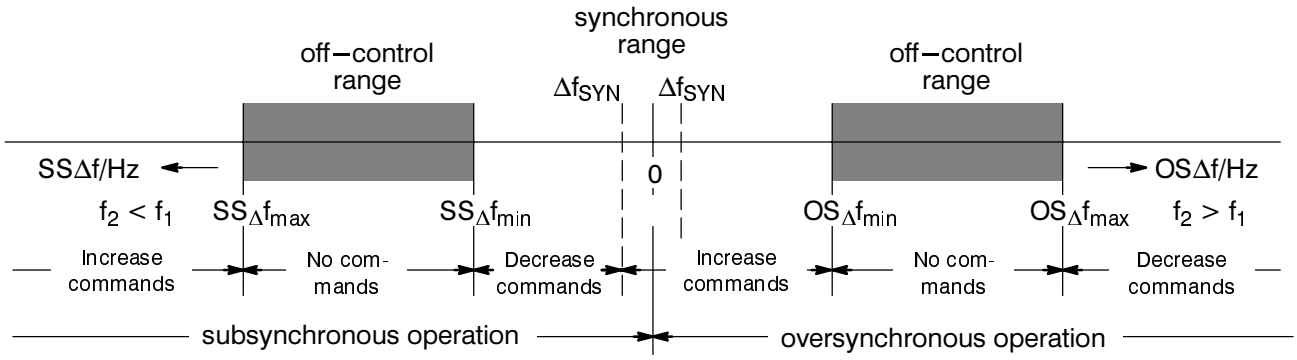
before start – frequency balancing commences just after connection of the auxiliary supply voltage

By energizing briefly the binary input ”Stop”, renewed balancing can be initiated

The frequency control outputs of 7VE512 can be used in two modes: In the balancing mode, they issue control commands for the speed regulator in order to adjust the frequency of the generator which is to be paralleled. In the status signal mode, the outputs indicate the status of the frequency. This section 6.3.7 is valid for the balancing mode. Proceed with Section 6.3.9 when the status mode is desired.

The off−control ranges (addresses 2319 to 2322) must first be defined for frequency balancing. Figure 6.4 shows the meaning of the four parameters. The frequency is no longer changed in the off−control range, the next synchronization point is calculated in advance in this case. The close command is output according to the parameterized closing time (address 2312). Outside the off−control ranges, the control commands shown in the figure are passed to the speed regulator.

No control pulses are given when the voltage phasors differ less than 180° from each other and are going to become synchronous. This applies, of course, only for that frequency range which is permissible for paralleling.



SSΔf : Frequency difference with subsynchronous operation $f_2 < f_1$

$SS\Delta f_{max}$: Frequency difference upper limit of off−control range

$SS\Delta f_{min}$: Frequency difference lower limit of off−control range

OSΔf : Frequency difference with oversynchronous operation $f_2 > f_1$

$OS\Delta f_{max}$: Frequency difference upper limit of off−control range

$OS\Delta f_{min}$: Frequency difference lower limit of off−control range

Figure 6.4 Setting ranges of the frequency balancer

No off−control range is present during oversynchronous operation, when the permissible frequency difference for oversynchronous switching (address 2107) is set to 0; i.e. in this case the machine is first controlled until it runs subsynchronous. Correspondingly, no subsynchronous off−control range is present when address 2108 is set to 0.

In the case of oversynchronous operation, the upper limit of the off−control range OS DEL f_{max} (address 2319) is set somewhat lower (e.g. 0.02 Hz) than the permissible frequency difference Δf with f2 > f1 (address 2307). If oversynchronous switching is not permitted (address 2307 set to 0 Hz), the limits of the off−control range for oversynchronous operation (addresses 2319 and 2320) have no significance. The frequency balancer then controls into the subsynchronous range in the case of oversynchronous operation.

In the case of subsynchronous operation, the upper limit of the off−control range SS DEL f_{max} (address 2321) is set somewhat lower (e.g. 0.02 Hz) than the permissible frequency difference Δf with f2 < f1 (address 2308). If subsynchronous switching is not permitted (address 2308 set to 0 Hz), the limits of the off−control range for subsynchronous operation (addresses 2321 and 2322) have no significance. The frequency balancer then controls into the oversynchronous range in the case of subsynchronous operation.

If neither oversynchronous nor subsynchronous switching is permitted, i.e. when both frequency difference limit values in addresses 2307 and 2308 are set to 0 Hz, the frequency difference will be regulated to 0. The device can then only give a close command under the conditions for synchronous switching.

Frequency balancing − upper limit of the off−control range for oversynchronous operation $f_2 > f_1$
Setting range: **0.01** Hz to **1.00** Hz

Frequency balancing − lower limit of the off−control range for oversynchronous operation $f_2 > f_1$
Setting range: **0.01** Hz to **1.00** Hz

Frequency balancing − upper limit of the off−control range for subsynchronous operation $f_2 < f_1$
Setting range: **0.01** Hz to **1.00** Hz

Frequency balancing − lower limit of the off−control range for subsynchronous operation $f_2 < f_1$
Setting range: **0.01** Hz to **1.00** Hz

The control duration factors and the pause duration factors are set in addresses 2323 to 2326 to adapt the control commands to the characteristic of the speed regulator. This is carried out separately for oversynchronous and subsynchronous operation. When the control duration factors SS Kc (address 2323) and OS Kc (address 2325) are set to 11, balancing is not possible. This setting is used only in the status mode as described in Section 6.3.9.

The control duration for subsynchronous operation is set in address 2323. The control direction depends on the actual frequency difference Δf outside the off−control range for subsynchronous operation (addresses 2321 and 2322). The relationship between the control duration factor Kc and the duration of the control command tc depending on the actual frequency difference Δf can be seen in Figure 6.5.

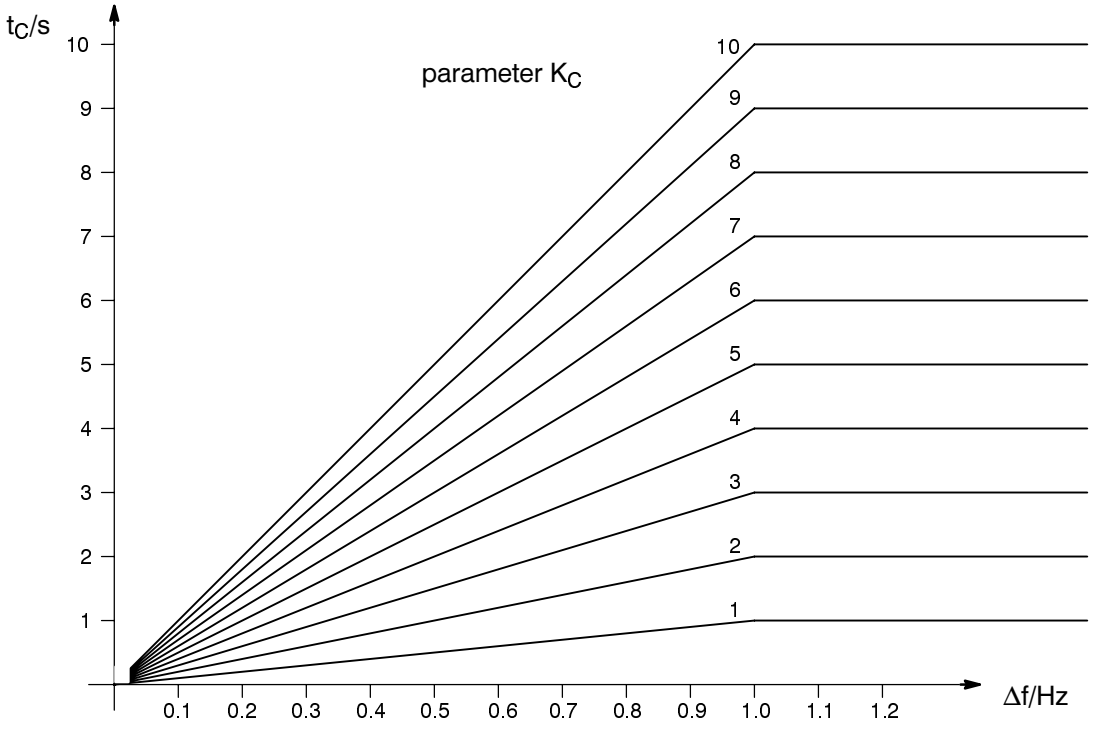


Figure 6.5 Frequency balancer – control duration

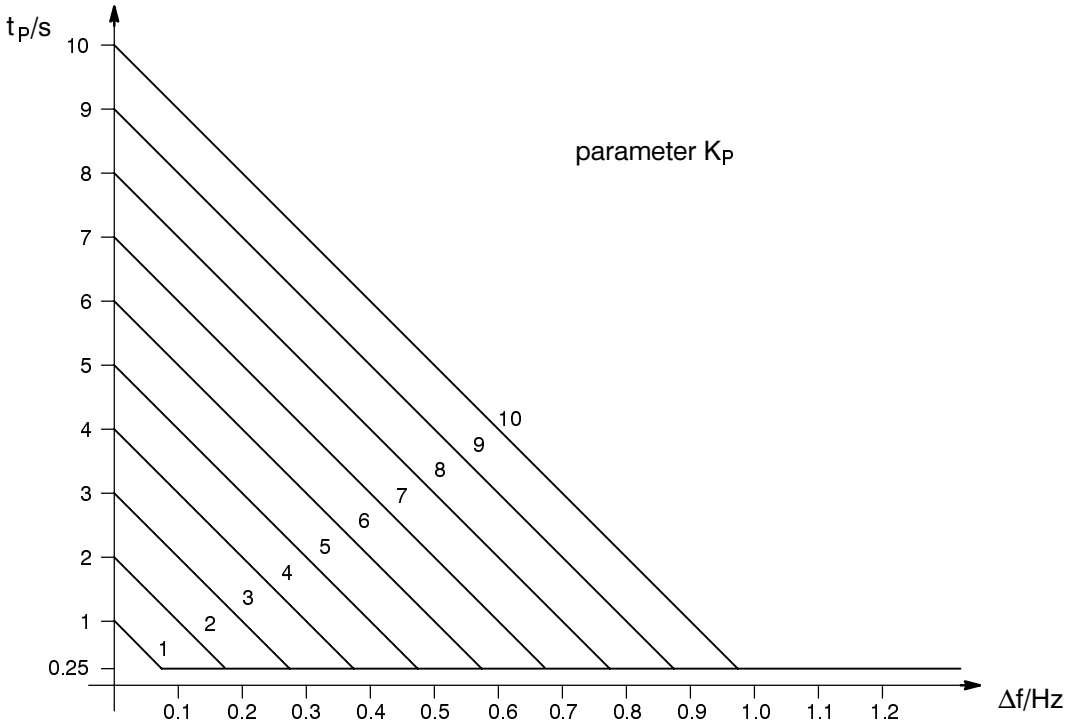
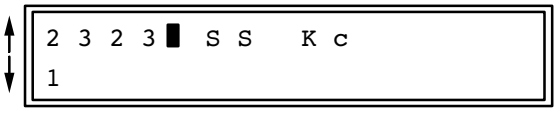
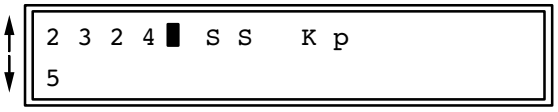


Figure 6.6 Frequency balancer – pause duration

The pause duration for subsynchronous operation is set in address 2324. The relationship between the pause duration factor Kp and the duration of the control pause tp depending on the actual frequency difference Δf can be seen in Figure 6.6. The minimum pause duration is 0.25 s.



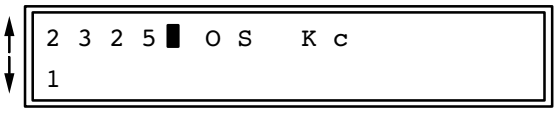
Frequency balancing – control duration factor for subsynchronous operation $f_2 < f_1$; refer diagram Figure 6.5
Setting range: **1** to **10**
(11 only for status indications, Section 6.3.9)



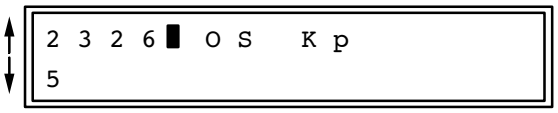
Frequency balancing – pause duration factor for subsynchronous operation $f_2 < f_1$; refer diagram Figure 6.6
Setting range: **1** to **10**

The control duration for oversynchronous operation is set in address 2325. The control direction depends on the actual frequency difference Δf outside the off–control range for oversynchronous operation (addresses 2319 and 2320). The relationship between the control duration factor Kc and the duration of the control command tc depending on the actual frequency difference Δf can be seen in Figure 6.5.

The pause duration for oversynchronous operation is set in address 2325. The relationship between the pause duration factor Kp and the duration of the control pause tp depending on the actual frequency difference Δf can be seen in Figure 6.6. The minimum pause duration is 0.25 s.

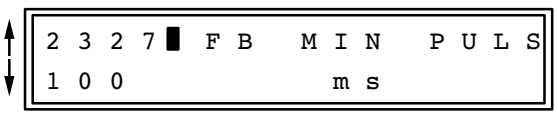


Frequency balancing – control duration factor for oversynchronous operation $f_2 > f_1$; refer diagram Figure 6.5
Setting range: **1** to **10**
(11 only for status indications, Section 6.3.9)



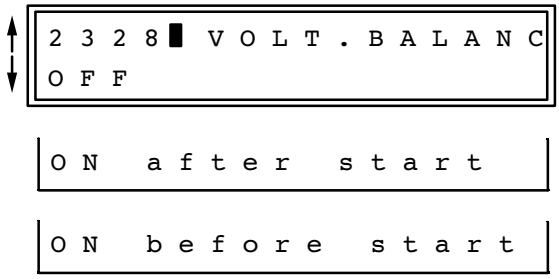
Frequency balancing – pause duration factor for oversynchronous operation $f_2 > f_1$; refer diagram Figure 6.6
Setting range: **1** to **10**

The minimum pulse duration for the control pulses can be set under address 2327. This definite minimum time cuts the characteristic at the transition between oversynchronous and subsynchronous operation and, thus, allows speedy regulation into the desired range.



Minimum puse duration for frequency balancing
Setting range: **30** ms to **300** ms

6.3.8 Settings for voltage balancing (7VE512 only)



Switching *ON*/*OFF* of the voltage balancer;

OFF – no voltage balancing

with *ON* a choice can be made:

after start – voltage balancing commences only after start command

before start – voltage balancing commences just after connection of the auxiliary supply voltage

By energizing briefly the binary input ”Stop”, renewed balancing can be initiated

---

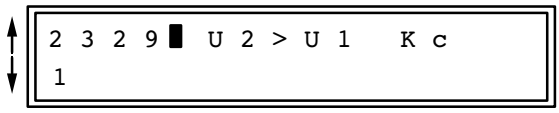
The voltage control outputs of 7VE512 can be used in two modes: In the balancing mode, they issue control commands for the voltage regulator in order to adjust the voltage of the generator which is to be paralleled. In the status signal mode, the outputs indicate the status of the voltage. This section 6.3.8 is valid for the balancing mode. Proceed with Section 6.3.9 when the status mode is desired.

The control duration factors and the pause duration factors are set in addresses 2329 to 2332 to adapt the control commands to the characteristic of the voltage regulator. This is carried out separately for a voltage drop and a voltage rise.

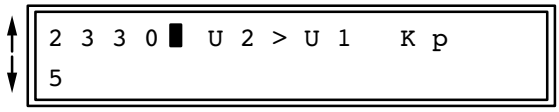
When the control duration factors U2>U1 Kc (address 2329) and U2<U1 Kc (address 2331) are set to 11, balancing is not possible. This setting is used only in the status mode as described in Section 6.3.9.

The control duration for U2 > U1 is set in address 2329. The direction of adjustment is ”U decrease”. The relationship between the control duration factor Kc and the duration of the control command tc depending on the actual voltage difference ΔU can be seen in Figure 6.7.

The pause duration for U2 > U1 is set in address 2330. The relationship between the pause duration factor Kp and the duration of the control pause tp depending on the actual voltage difference ΔU can be seen in Figure 6.8. The minimum pause duration is 0.25 s.



Voltage balancing – control duration factor for ”U2 decrease” (U2 > U1); refer diagram Figure 6.7
Setting range: **1** to **10**
(11 only for status indications, see Section 6.3.9)



Voltage balancing – pause duration factor for ”U2 decrease” (U2 > U1); refer diagram Figure 6.8
Setting range: **1** to **10**

The control duration for U2 < U1 is set in address 2331. The direction of adjustment is ”U increase”. The relationship between the control duration factor Kc and the duration of the control command tc depending on the actual voltage difference ΔU can be seen in Figure 6.7.

The pause duration for U2 < U1 is set in address 2330. The relationship between the pause duration factor Kp and the duration of the control pause tp depending on the actual voltage difference ΔU can be seen in Figure 6.8. The minimum pause duration is 0.25 s.

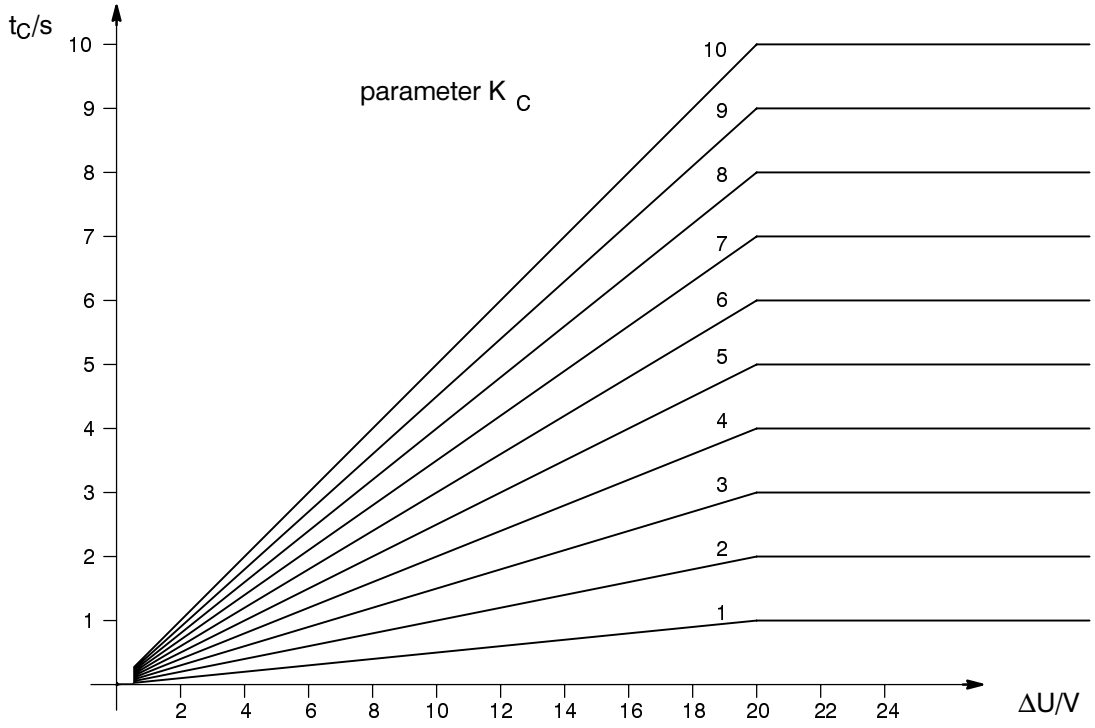


Figure 6.7 Voltage balancer – Control duration

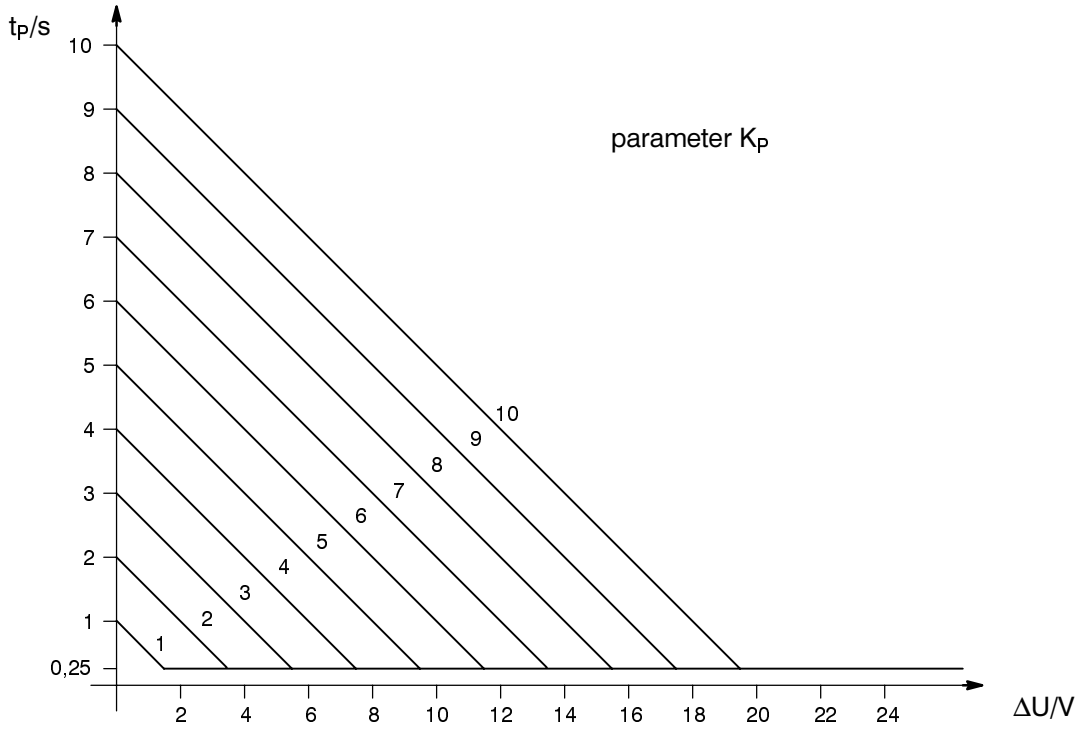
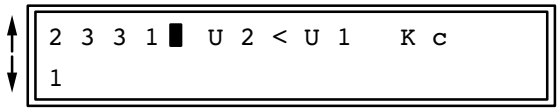
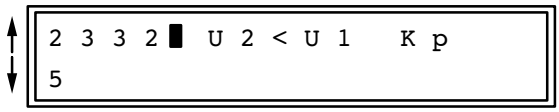


Figure 6.8 Voltage balancer – pause duration

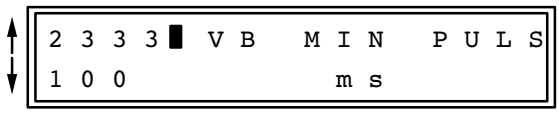


Voltage balancing – control duration factor for "U2 increase" (U2 < U1); refer diagram Figure 6.7
Setting range: **1** to **10**
(11 only for status indications, see Section 6.3.9)



Voltage balancing – pause duration factor for "U2 increase" (U2 < U1); refer diagram Figure 6.8
Setting range: **1** to **10**

The minimum pulse duration for the control pulses can be set under address 2333. This definite minimum time cuts the characteristic at the transition between oversynchronous and subsynchronous operation and, thus, allows speedy regulation into the desired range.



Minimum puse duration for voltage balancing
Setting range: **30** ms to **300** ms

6.3.9 Output of status signals (7VE512 only)

The frequency and voltage control outputs of 7VE512 can be used in two modes: In the balancing mode, they issue control pulses for the speed and voltage regulator in order to adjust the frequency and voltage of the generator which is to be paralleled. In the status signal mode, the outputs indicate the status of the frequency, voltage, and phase angle difference. This section 6.3.9 is valid for the status mode. When frequency and voltage balancing is required, refer to the sections 6.3.7 and 6.3.8.

The mode must be the same for one parameter set but may be different for a different parameter set.

Figure 6.9 illustrates the frequency difference ranges in which the frequency signals are issued:

F2 >> when the frequency f2 is too high,
F2 << when the frequency f2 is too low.

The frequency f1 must be in the operating range 47.5 Hz $\leq$ f1 $\leq$ 52.5 Hz for f_N = 50 Hz, or 57.0 Hz $\leq$ f1 $\leq$ 63.0 Hz for f_N = 60 Hz, as stated in the Technical data (Section 3.1.1).

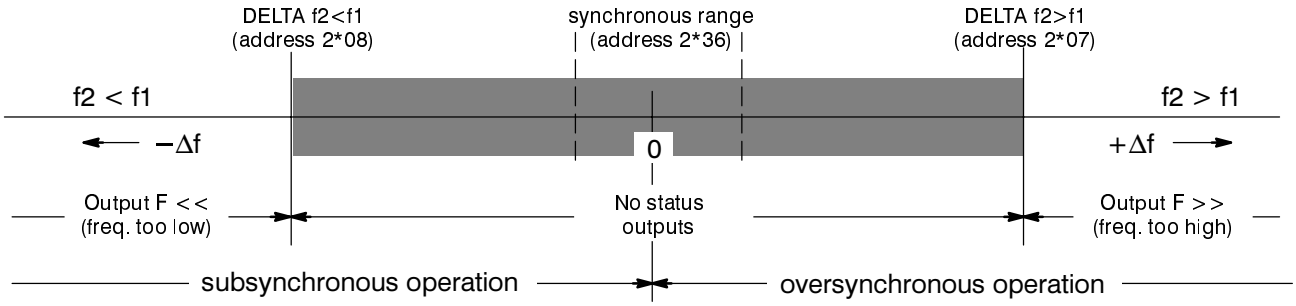


Figure 6.9 Status signals in the frequency range

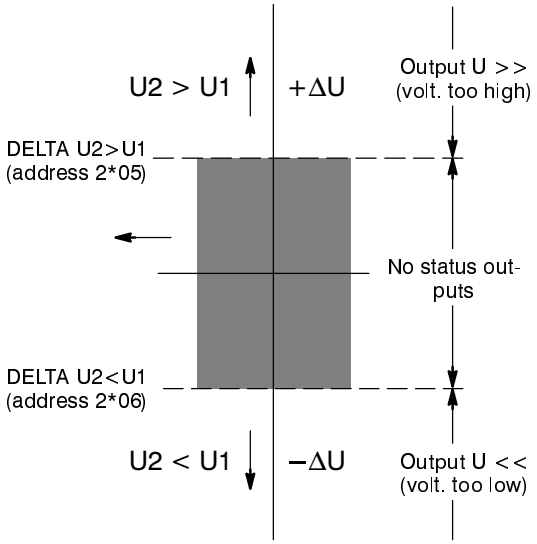


Figure 6.10 Status signals in the voltage range

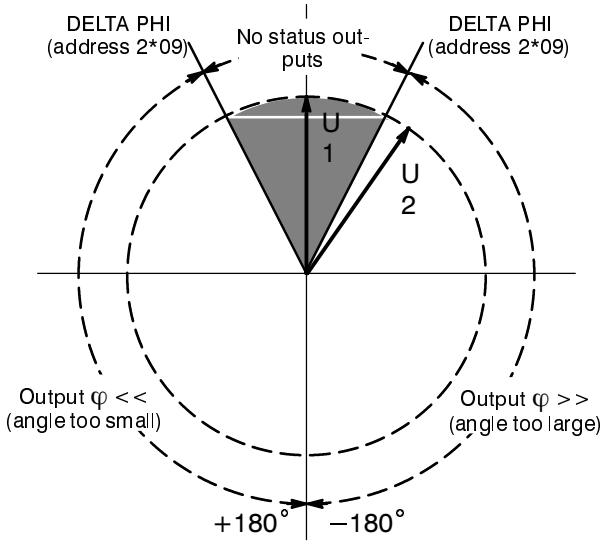


Figure 6.11 Status signals in the angle range

No signals are issued within the permissible frequency range as set under addresses 2*07 and 2*08 (see Section 6.3.6; the "*" represent the parameter set).

Similarly, the voltage status signal are generated as illustrated in Figure 6.10:

U2 >> when the voltage U2 is too high,
U2 << when the voltage U2 is too low.

The voltage U1 must lie within the limits as parameterized under addresses 2*01 and 2*02 (see Section 6.3.5).

No signals are issued within the permissible voltage range as set under addresses 2*05 and 2*06 (see Section 6.3.6; the "*" represent the parameter set).

The phase angle status signals are generated according the illustration in Figure 6.11:

φ >> too	when the angle between U2 and U1 is large and positive (U2 leading),
φ << too	when the angle between U2 and U1 is large and negative (U2 lagging).

Address 2318 determines at what time the status signals are output. *OFF* means no status outputs. Two possibilities exist for the *ON*–condition: generation of the status signals may commence *after start*, i.e. after the start signal is registered by the relay, or *before start*, i.e. as soon as the relay is switched on and operative.

The control duration factors SS Kc (address 2323 for oversynchronous operation) and OS Kc (address 2325 for subsynchronous operation) must **both** be set to **11** when the status signal mode is used!

Address 2328 determines at what time the status signals are output. This setting must be equal to the setting of address 2318.

The limits of voltage difference have already been set under addresses 2305 and 23306 (see Section 6.3.6).

The control duration factors U2>U1 Kc (address 2329) and U2<U1 Kc (address 2331) must **both** be set to **11** when the status signal mode is used!

Note: The four duration factors SS Kc (address 2323), OS Kc (address 2325), U2>U1 Kc (address 2329) and U2<U1 Kc (address 2331) must all be set to 11 for status signal mode even when one of the status outputs is not used or address 2318 and/or 2328 are set *OFF*!

The remaining addresses are used only in the balancing mode (Section 6.3.7 and 6.3.8).

```
2318 FREQ. BALANC
OFF
```

```
ON after start
```

```
ON before start
```

Switching *ON*/*OFF* of the status signals;

OFF – no status signals

with *ON* a choice can be made:

after start – status signals commence only after start command

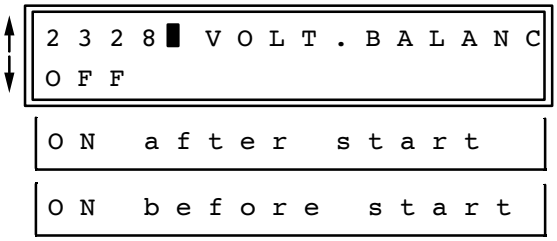
before start – status signals commence just after connection of the auxiliary supply voltage

```
2323 SS Kc
1
```

Control duration factor for subsynchronous operation $f_2 < f_1$
must be set to 11 for status indications

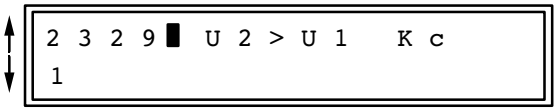
```
2325 OS Kc
1
```

Control duration factor for oversynchronous operation $f_2 > f_1$
must be set to 11 for status indications

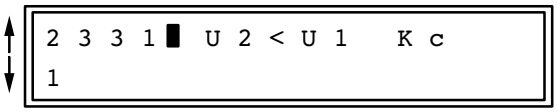


Switching *ON*/*OFF* of the status signals

setting must be equal to that of address 2318



Control duration factor for U2 > U1
must be set to 11 for status indications



Control duration factor for U2 < U1
must be set to 11 for status indications

6.4 Annunciations

6.4.1 Introduction

After synchronization, annunciations and messages provide a survey of the function of the device, and serve for checking sequences of functional steps during testing and commissioning. Further, they provide information about the condition of measured data and the device itself during normal operation.

To read out recorded annunciations, no codeword input is necessary.

The annunciations generated in the device are presented in various ways:

– LED indications in the front plate of the device (Figure 6.1 or 6.2),

– Binary outputs (output relays) via the connections of the device,

– Indications in the display on the front plate or on the screen of a personal computer, via the operating interface,

To call up annunciations on the operator device, the following possibilities exist:

– Block paging with the keys ⇑ forwards or ⇓ backwards up to address 5000,

– Direct selection with address code, using key **DA**, address **5 0 0 0** and execute with key **E**,

– Press key **M**/**S** (M stands for ”messages”, S for ”signals”); then the address 5000 appears automatically as the beginning of the annunciation blocks.

Block 51 Operational annunciations; these are messages which can appear during the operation of the device: information about conditions of device functions; measurement data etc.

Block 52 Annunciations for the last paralleling procedure; start, condition of ΔU, Δf, $\Delta\varphi$, control and closing command, or similar.

Block 53 Annunciations for the previous paralleling procedure, as block 52.

Block 54 Annunciations for the last but two paralleling procedure, as block 52.

Block 57 Indication of operational measured values (voltages, frequencies, differences, phase rotation).

Commencement of ”annunciation blocks”

A comprehensive list of the possible annunciations and output functions with the associated function number FNo is given in Appendix C. It is also indicated to which device each annunciation can be routed.

6.4.2 Operational annunciations on the display or via the operating interface – address block 51

Operational annunciations contain information which the unit provides during operation and about the operation. They begin at address 5100. Important events and status changes are chronologically listed, starting with the most recent message. Time information is shown in minutes. Up to 30 operational indications can be stored. If more occur, the oldest are erased in sequence.

The input of the codeword is not required. After selection of the address 5100 (by direct selection with **DA 5 1 0 0 E** and/or paging with ⇑ or ⇓ and further paging with ↑ or ↓) the operational annunciations appear. The boxes below show all available operational annunciations following the box with the main block heading. In each specific case, of course, only the associated annunciations appear in the display.

Next to the boxes below, the abbreviated forms are explained. It is indicated whether an event is announced on occurrence (**C** = "Coming") or a status is announced "Coming and Going" (**C**/**G**). The first listed message is, as example, the begin of the condition and the following line gives the consecutive number and relative time (from the last restart).

5100 OPERATIONAL ANNUNCIATIONS	Beginning of the blocks "Operational annunciations"
SYNCHR. 5 →	Paralleling in progress, general (C/G)
n 000 68 min	Example for consecutive No. and relative time
LED-reset	LED reset or tested (C)
Failure 15V	Failure 15 V internal supply voltage (C/G)
Failure 0V	Failure 0 V analog/digital converter (C/G)
Failure 24V	Failure 24 V internal supply voltage (C/G)
Failure 5V	Failure 5 V internal supply voltage (C/G)
Failure GEA	Failure command relay on basic input/output module GEA (C/G)
Failure ZEA	Failure command relay on additional input/output module ZEA (only 7VE512) (C/G)
Par. running	Parameters are being set (C/G)
ParSelec.Flt	Faulty selection of a parameter block (no or more than 1 parameter set selected) (C/G)
Par.Data Flt	Parameter data faulty (C)
Re-start	Re–start annunciation of the processor system (C)
Initial.Flt	Fault during initialization of the processor system (C)
PhaseSeq.Flt	Phase sequence wrong (C)

NO SET SELEC	No parameter set has been selected; when longer than 5 sec
SET SELEC. 1	Parameter set 1 is selected
SET SELEC. 2	Parameter set 2 is selected
SET SELEC. 3	Parameter set 3 is selected
SET SELEC. 4	Parameter set 4 is selected
SET SELEC. 5	Parameter set 5 is selected
SET SELEC. 6	Parameter set 6 is selected
[Table empty]	If not all storage places are used, the remaining are indicated as *empty*

6.4.3 Annunciations concerning paralleling procedure – address blocks 52 to 54

The annunciations which occurred during the last three paralleling procedures can be read off. The indications are recorded in the sequence from the youngest to the oldest under address 5200, 5300 and 5400. With a new paralleling procedure, the data relating to the oldest are erased. Input of the codeword is not required.

To call up the data of the **last** paralleling procedure, one goes to address 5200 either by direct address **DA** or by paging with the keys ⇑ or ⇓. With the keys ↑ or ↓ one can page the individual annunciations forwards or backwards.

In the following clarification, all the available annunciations for paralleling are attached to the block with the main address. In a specific case, of course, only the associated annunciations appear in the display.

⇑ 5200 LAST SYNCHRONIZATION ⇓	Beginning of the blocks "Last synchronization"
SYNCHR. No 5	Consecutive No. n of the paralleling procedure (e.g. 5)
(time) started	Paralleling procedure started
started: S 1	Paralleling started with parameter set 1
started: S 2	Paralleling started with parameter set 2
started: S 3	Paralleling started with parameter set 3
started: S 4	Paralleling started with parameter set 4
started: S 5	Paralleling started with parameter set 5
started: S 6	Paralleling started with parameter set 6

A b o r t e d	Paralleling procedure aborted (e.g. because of wrong phase sequence or parameter data fault)
D e l t a U > >	Voltage magnitude difference ΔU too large
D e l t a U o k	Voltage magnitude difference ΔU within the set limits
D e l t a F > >	Frequency difference Δf too large
D e l t a F o k	Frequency difference Δf within the set limits
P h i > >	Phase angle difference Δφ too large
P h i o k	Phase angle difference Δφ within the set limits
U 1 U 2 s y n c h	Voltages are synchronous (for synchronous paralleling)
U 1 U 2 a s y n c	Voltages are asynchronous (for asynchronous paralleling)
F a i l . U m e a s	Measured voltages faulty (e.g. failure of a voltage)
S t o p p e d	Paralleling stopped (e.g. via binary input)
T s y n S T A R T	Synchronizing time started
T s y n S T O P	Synchronizing time stopped
T s y n o v e r	Permissible synchronizing time expired
S y n c . > 1 m i n	Synchronization condition longer than 1 minute

Status annunciations:

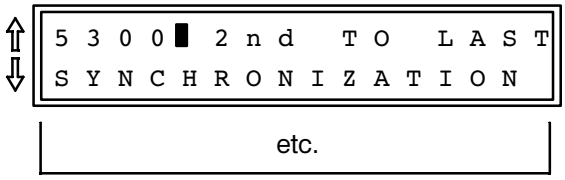
U 1 > >	Voltage magnitude U1 too large
U 1 < <	Voltage magnitude U1 too small
U 2 > >	Voltage magnitude U2 too large
U 2 < <	Voltage magnitude U2 too small
F 1 > >	Frequency f1 too large
F 1 < <	Frequency f1 too small
F 2 > >	Frequency f2 too large
F 2 < <	Frequency f2 too small

Command annunciations:

Close1 Cmd	Closing command given by the envelop curve measuring algorithm (method 1)
Close1 res	Reset of closing command 1
Close2 Cmd	Closing command given by the zero crossing measuring algorithm (method 2)
Close2 res	Reset of closing command 2

Table empty	means, no paralleling data are recorded (yet)
Table overflow	means, further data had been announced but are lost because of memory overflow
Table superceded	a new paralleling procedure occurred during read–out of data; leave the block and call it up again

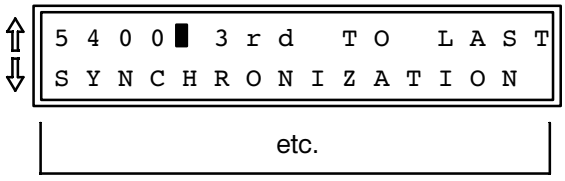
The data of the **second to last** synchronization can be found under address 5300. The available annunciations are the same as for the last synchronization.



Beginning of block " Second to last synchronization"

etc.

The data of the **third to last** synchronization can be found under address 5400. The available annunciations are the same as for the last synchronization.



Beginning of block "Third to last synchronization"

etc.

6.4.4 Annunciations on LED indicators and output signal relays

The unit 7VE511 contains 8 LEDs, model 7VE512 contains 16 LEDs for optical indications on the front. Front views are illustrated in Figures 6.1 and 6.2 (Section 6.2.4). Table 6.1 lists the meanings of the indications for model 7VE511, valid also for the basic input/output module of model 7VE512.

LED	Designation	Color	Meaning
	Betrieb/Service	green	Device is in service
	Störung/Blocked	red	Device is blocked: internal fault detected
1	Ein A/Closing A	red	Closing command 1 (1st channel) present
2	Ein B/Closing B	red	Closing command 2 (2nd channel) present
3	Angeregt/Started	red	Device is started, extinguishes with closing command or when aborted
4	$\Delta f <$	red	Frequency difference within the permissible limits
5	$\Delta U <$	red	Voltage difference within the permissible limits
6	$\varphi <$	red	Angle difference within the permissible limits (synchronous switching)

Table 6.1 LEDs on basic input/output module (7VE511 and 7VE512)

The LED 6 flashes during parameterizing. When pushing the button ”RESET LED” on the front of the device, all LEDs are illuminated. Thus, the LEDs are tested. This push−button can be accessed when the cover is closed.

The indications on the additional input/output module of model 7VE512 are listed in Table 6.2. The meaning of LED 8 to LED 11 depends on the selected synchronization mode. In balancing mode, they indicate the control commands, in status mode, they indicate the status of the measured values.

LED	Designation	Color	Meaning
7	Abwurf/Stop	red	illuminated for at least 3 s after reception of a stop signal
8	f↑	red	illuminated during control command ”increase frequency” (balanc.) illuminated during status ”frequency too high” (status)
9	f↓	red	illuminated during control command ”decrease frequency” (balanc.) illuminated during status ”frequency too low” (status)
10	U↑	red	illuminated during control command ”increase voltage” (balanc.) illuminated during status ”voltage too high” (status)
11	U↓	red	illuminated during control command ”decrease voltage” (balanc.) illuminated during status ”voltage too high” (status)
12	$\Delta f <<$	red	illuminated during synchronism, i.e. $\Delta f <$ DELTA f SYN (2*36)
13	$1 \neq 2$	red	phase sequence wrong or measured voltage faulty
14	Sync./block.	red	synchronization blocked

Table 6.2 LEDs on additional input/output module (7VE512 only)

The allocation of the signal output relays is shown in the connection diagrams in appendix B and explained in the following table.

Alarm relay ”Device fault” indicates a disturbance by drop−off of the NC contact. When the auxiliary voltage is absent, the relay drops off. With auxiliary voltage present, the relay is de−exited when the device has detected an internal fault. If the paralleling device is switched to auxiliary supply only during the paralleling procedure, external measures are to be taken to avoid that the alarm of this relay output is interpreted as ”Device fault”.

Relay	Annunciation	Meaning
1	Sync. in progress	comes when the relay has accepted a start command, goes when the relay is stopped or has stopped itself.
2	Sync. blocked	comes when the relay is blocked after activation, comes 5 s after a parameter selection fault has been detected, goes when the relay is stopped or when the selection fault is removed.
3	Device fault	NO contact is closed when the relay is operative (normal operation), NC contact is closed with missing auxiliary voltage or when a hardware or software fault has been detected.

Table 6.3 Signal relays (7VE511 and 7VE512)

The remaining relays are available only in model 7VE512. They are listed in Table 6.4. The meaning depends on the selected synchronization mode. In balancing mode, they indicate the control commands, in status mode, they indicate the status of the measured values.

Relay	Annunciation	Meaning
4	Phi >>	angle difference φ too large (φ positive, only status mode);
5	Phi >>	angle difference φ too large (φ negative, only status mode);
6	F2 >>	control command ”increase frequency” (balancing mode), frequency too high (status mode);
7	F2 <<	control command ”decrease frequency” (balancing mode), frequency too low (status mode);
8	U2 >>	control command ”increase voltage” (balancing mode), voltage too high (status mode);
9	U2 <<	control command ”decrease voltage” (balancing mode), voltage too low (status mode);
10	Fail.Umeas	Measured voltage failure (independent on mode)

Table 6.4 Signal relays (7VE512 only)

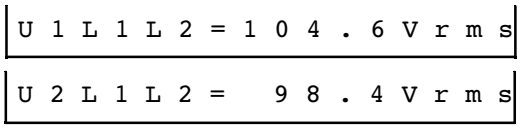
6.4.5 Read–out of operational measured values – address block 57

The steady state r.m.s. operating values can be read out at any time under address **57**00. The address can be called–up directly using **DA 5 7 0 0 E** or by paging with ⇑ or ⇓. The individual measured values can be found by further paging with ↑ or ↓. Entry of the codeword is not necessary. During the read–out procedure the values will be updated. When paralleling is in progress the update rate will be slower.

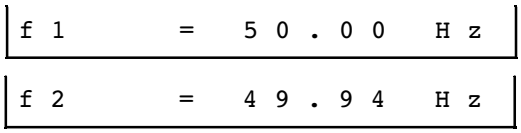
In the following example, some typical values have been inserted. In practice, the actual values appear. The possible ranges are given in text at the right of the blocks.

Address 5800 shows dynamic measured values which appear during synchronization and can be read out.

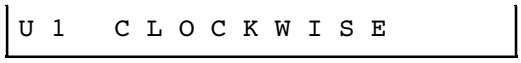
Beginning of the blocks "Operational measured values"



Voltages $U1_{L1-L2}$ and $U2_{L1-L2}$
Range **0** V to **140** V

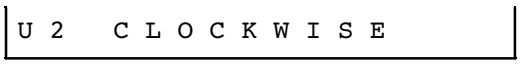


frequencies f1 and f2
Range **35** Hz to **70** Hz

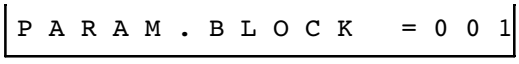


Phase rotation of voltage U1, provided $U1_{L2-L3}$ is connected:

CLOCKWISE/*COUNTER–CLOCK*wise – measured phase rotation
W/O PH.SEQ. – without phase sequence check: Voltage U_{L2-L3} not connected or voltage too small
WRONG PH.SEQ. – wrong phase sequence



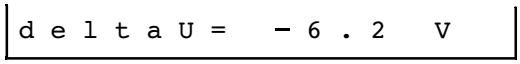
Phase rotation of voltage U2, provided $U2_{L2-L3}$ is connected
messages as for U1



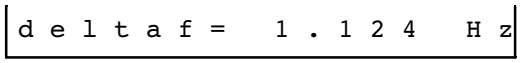
Set of parameters (parameter block) which is valid with **7VE511**:
PARAM.BLOCK = 001 relates to addresses 21★★
PARAM.BLOCK = 002 relates to addresses 22★★

with **7VE512**:
PARAM.BLOCK = 001 relates to addresses 23★★
PARAM.BLOCK = 002 relates to addresses 24★★
PARAM.BLOCK = 003 relates to addresses 25★★
PARAM.BLOCK = 004 relates to addresses 26★★
PARAM.BLOCK = 005 relates to addresses 27★★
PARAM.BLOCK = 006 relates to addresses 28★★

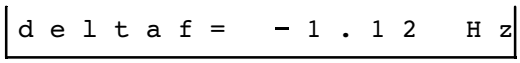
Beginning of the blocks ”Operational measured values”



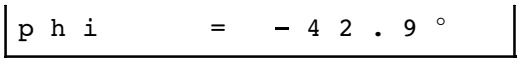
Voltage difference U2−U1
Range **0** V to **140** V



Frequency difference f2−f1
Range **0** Hz to **30** Hz



(negative values are truncated to 2 decimals)



Angle difference φ2−φ1
Range **−180**° to **+180**°

6.5 Commissioning

6.5.1 General

Prerequisite for commissioning is the completion of the preparation procedures detailed in Chapter 5.

Warning

Hazardous voltages are present in this electrical equipment during operation. Non−observance of the safety rules can result in severe personal injury or property damage.

Only qualified personnel shall work on and around this equipment after becoming thoroughly familiar with all warnings and safety notices of this manual as well as with the applicable safety regulations.

Particular attention must be drawn to the following:

- The earthing screw of the device must be connected solidly to the protective earth conductor before any other connection is made.
- Hazardous voltages can be present on all circuits and components connected to the supply voltage or to the measuring and test quantities.
- Hazardous voltages can be present in the device even after disconnection of the supply voltage (storage capacitors!).
- The limit values given in the Technical data (Section 3.1) must not be exceeded at all, not even during testing and commissioning.

During working on this device, no further measuring quantities must be present and all control outputs must be interrupted.

Warning

Primary tests shall be performed only by qualified personnel which is familiar with the particular requirements concerning synchronizing equipment and with the operation of the machine or switchgear as well as the rules and regulations (switching, earthing, etc.).

The procedure described below must therefore not be considered as complete commissioning instructions but only indicates the necessary steps using examples. The individual possibilities and requirements of the switch gear must be observed in addition.

Primary tests comprise the following steps:

– Checking the control circuits,
– Checking the measured voltage circuits,
– Measuring the circuit breaker close times,
– Dummy synchronization attempt,
– Operational paralleling.

6.5.2 Checking the control circuits

The adjacent isolators are open when the circuit breaker is checked. Check that the circuit breaker can only be closed by activating the discrepancy switch if the synchronizing switch (if present) is in the position ”Manual”, and only by the paralleling device if the switch is in the position ”Automatic”.

In the model 7VE512 (with frequency and voltage balancers), the correct reaction of the voltage and speed regulators to the control commands (increase/decrease) is checked from the paralleling device.

When the status mode is selected, check that the signal outputs are correctly connected. *Note* that the meaning of the status signals is different from that of the balancing control signals e.g.:

f↑ in balancing mode means: frequency must be increased,

f>> in status mode means: frequency is too high.

The above−mentioned tests are carried out for each paralleling location if several of these are present. All associated circuit breakers are isolated on both sides as far as possible in order to check the assignment between the selected paralleling location and the circuit breaker.

6.5.3 Checking the measured voltage circuits

The phase sequences and connection of the voltages to be paralleled must be checked. The checks may be carried out in different manners depending on the assignment of the voltage transformers.

If the synchronize location has voltage transformers to both sides of the circuit breaker (Figure 6.12), the voltage checks can be carried out simply on these voltage transformers:

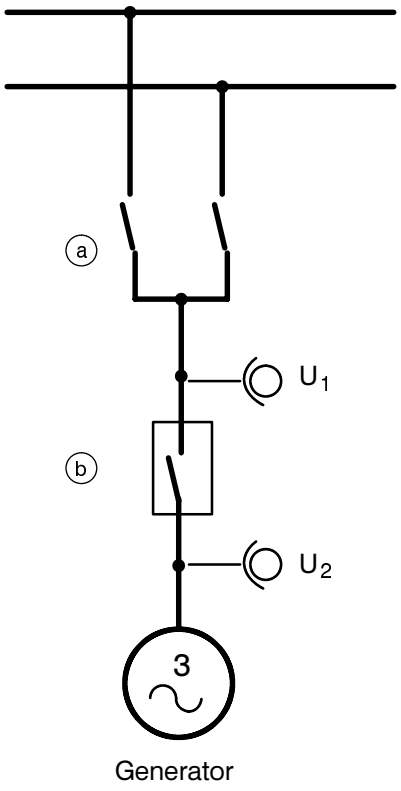


Figure 6.12 Measured voltages for synchronizing

With the circuit breaker (b) open, the voltage transformer on the bus−bar side is powered by the network: close isolator (a).

The voltage is read out on the paralleling device in the operational measured values under address 5700 as *U1L1L2* and compared with the actual voltage. Note that the displayed measured voltage U1 is influenced by the matching factor U2/U2, too.

The phase sequence is subsequently checked. If two phase−to−phase voltages are connected on the device, the phase rotation can also be read out in the operational measured values under address 5700 as *U1 CLOCKWISE* or *U1 COUNTER−CLOCK*. The secondary wiring to the paralleling device is also checked in this manner.

Open bus−bar isolator (a).

The generator voltage in the 7VE51 is read out in the operational measured values under address 5700 as *U2L1L2* after running−up the generator and compared with the actual voltage.

The phase sequence check is subsequently carried out with the generator voltage: the phase sequence of the generator voltage must be the same as that of the network voltage. If two phase−to−phase voltages are connected on the device, the phase rotation can be read out in the operational measured values under address 5700 as *U2 CLOCKWISE* or *U2 COUNTER CLOCK*. The secondary wiring to the paralleling device is checked in this manner.

Subsequent checking of the secondary voltage circuits is carried out in that identical voltages are applied to the two voltage transformers. The generator feeder must be isolated from the bus−bar. The circuit breaker (b) is closed so that the two voltages U1 and U2 are identical.

Convince yourself using the operational measured values of the 7VE51 under address 5700 that, within the measured tolerances
- the two voltages *U1L1L2* and *U2L1L2* are the same,
- the two frequencies *f1* and *f2* are the same,
- the voltage difference *deltaU* is zero,
- the frequency difference *deltaF* is zero,
- the angle difference *phi* is zero.

The 7VE51 carries out a phase sequence check if two phase−to−phase voltages are connected to it; the same phase sequence must be indicated under address 5700 for both voltages:
- *U1* phase sequence equal to *U2* phase sequence.

In the case of several paralleling locations, the examination must be carried out for each location if the voltages also change together with the locations.

In the case of bus–bar voltage transformers, check the voltage applied to the device via the isolator auxiliary contacts for each bus–bar if applicable by reading the operational measured values (address 5700) and comparing with the actual voltage. Connect each of the bus–bar voltages to the measuring point in succession by switching over the isolators or by temporarily shorting the isolator auxiliary contacts.

An arrangement as in Figure 6.13 enables voltage checks to be carried out both for the network voltage and for the generator voltage in the measuring bay. **Only one of the circuit breakers (a) or (b) must be closed at a time!** The network voltage is present in the measuring bay with the generator breaker (b) open and the bus–tie breaker (a) closed. The generator voltage can be checked by opening the bus–tie breaker (a) and closing the generator breaker (b).

First carry out voltage checks with the network voltage; (b) open, (a) closed. The voltage is read out on the paralleling device in the operational measured values under address 5700 as *U1L1L2* and compared with the actual voltage. Note that the displayed measured voltage U1 is influenced by the matching factor U2/U2, too.

The phase sequence is subsequently checked. If two phase–to–phase voltages are connected on the device, the phase rotation can also be read out in the operational measured values under address 5700 as *U1 CLOCKWISE* or *U1 COUNTER CLOCK* and compared with the phase rotation determined in the measuring bay. The secondary wiring to the paralleling device is also checked in this manner.

Subsequently **open the bus–tie breaker (a) again.**

The phase sequence check is carried out with the generator voltage after running–up the generator; (a) open, (b) closed. The voltage can be read out in the 7VE51 in the operational measured values under address 5700 as *U1L1L2* and compared with the actual voltage.

The phase sequence of the generator voltage must be equal to that of the network voltage. If two phase–to–phase voltages are connected on the device, the phase rotation can be read out in the operational measured values under address 5700 as *U1 CLOCKWISE* or *U1 COUNTER CLOCK* and compared with the phase rotation determined in the measuring bay. The secondary wiring to the paralleling device is also checked in this manner.

Subsequently **open breaker (b) again.**

Subsequent checking of the secondary voltage circuits is carried out in that identical voltages are applied to the two voltage transformers. The bus–tie breaker (a) must be open so that a network voltage is not present. The generator breaker (b) is closed so that the voltages U1 and U2 applied to the device are identical.

Convince yourself using the operational measured values of the 7VE51 under address 5700 that, within the measured tolerances

– the two voltages *U1L1L2* and *U2L1L2* are the same,

– the two frequencies *f1* and *f2* are the same,

– the voltage difference *deltaU* is zero,

– the frequency difference *deltaF* is zero,

– the angle difference *phi* is zero.

The 7VE51 carries out a phase sequence check if two phase–to–phase voltages are connected to it; the same phase sequence must be indicated under address 5700 for both voltages:
– *U1* phase sequence equal to *U2* phase sequence.

In the case of several bus–bars, the examination must be carried out for each bus–bar voltage.

In the case of several paralleling locations, the examination must be carried out for each location if the voltages also change together with the locations.

The above–mentioned applies accordingly to the paralleling of networks. Figure 6.14 shows a possible connection arrangement.

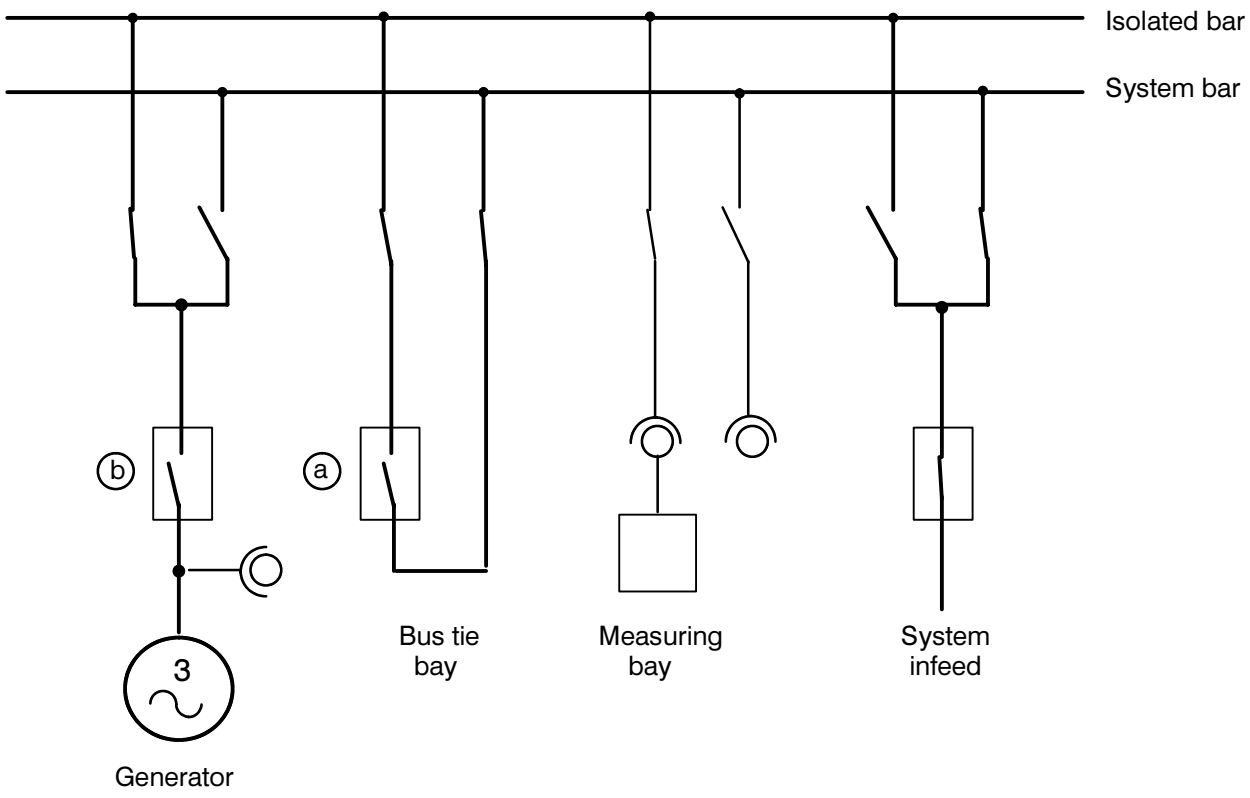


Figure 6.13 Checking the measured voltages in the measuring bay or section – example

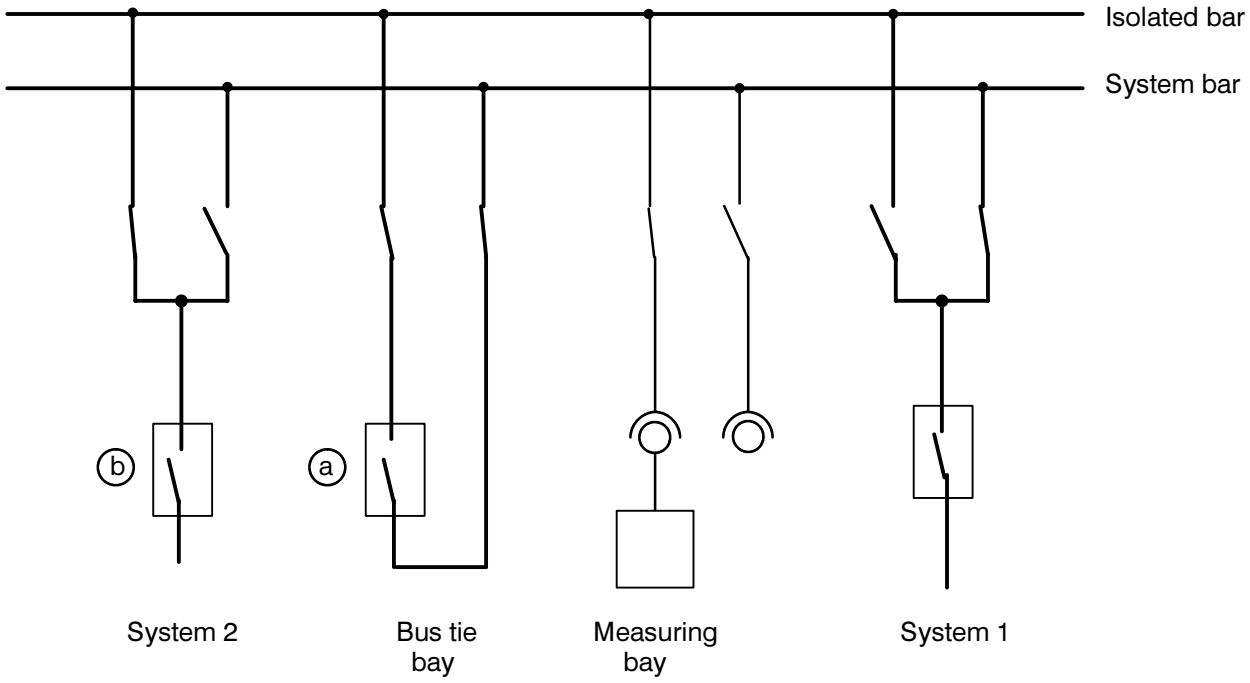


Figure 6.14 Checking the measured voltages in the measuring bay or section – example

6.5.4 Measuring the closing time of the circuit breaker

In order to achieve exact paralleling with phase angle 0, the breaker operating time must be measured when closing and set correctly in address 2⋆12 (see also Section 6.3.6). The experimental arrangement varies depending on the switch gear configuration, but should correspond to the basic idea that the steady−state voltage present on a voltage transformer (U2) is switched via the circuit breaker to a second voltage transformer (U1) (Figure 6.15). **The voltage U1 must be isolated from the network during the process!**

The time meter must be set to the 1−s range or to a resolution of 1 ms.

Close the circuit breaker manually; the time meter is started at the same time. The voltage U1 appears when the poles of the circuit breakers are closed; the time meter is then stopped. The time indicated on the meter is the circuit breaker closing time.

The experiment must be repeated if the time meter does not stop because of an unfavourable closing instant.

It is best to calculate the mean value from several (3 to 5) successful switching attempts and to set this under address 2⋆12 CB CLOSE TM (see also Section 6.3.6).

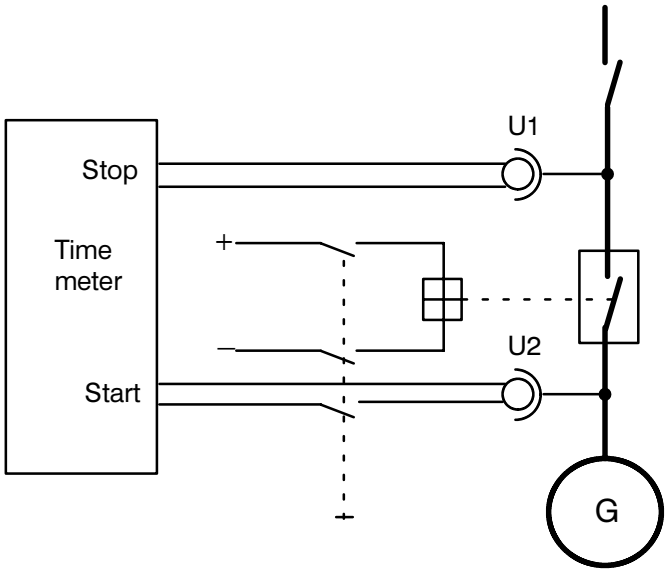
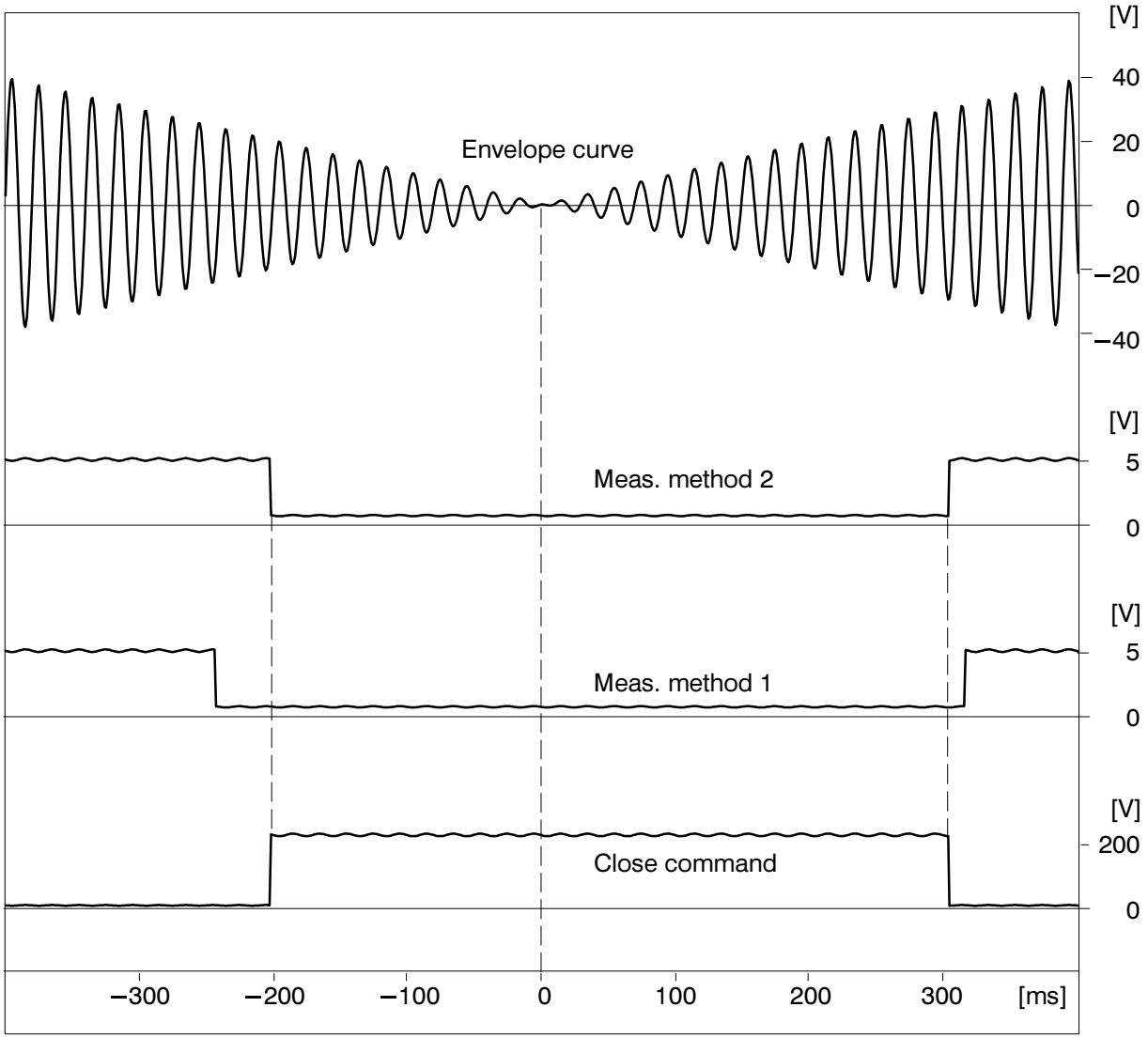


Figure 6.15 Measuring the circuit breaker closing time

6.5.5 Dummy synchronization attempts



Set parameters		Measured values	
Delta f2 > f1	1.01 Hz	Frequency difference	+ 200 mHz
Delta f2 < f1	1.01 Hz	System frequency	50 Hz
Delta Phi	8 deg.	Command duration	505 ms
Angle window	3 deg.	Angle error	0.14 deg.
CB Close Time	200 ms	Switching angle	14.4 deg.
Command duration	500 ms		

Figure 6.16 Dummy synchronization sequence, example

The setting values should be checked again (see Section 6.3).

Switch off the circuit breaker. The close command to the circuit breaker as well as any control commands must be interrupted (disconnection of close and control commands). Switch through the network voltage for the measurement.

Set the generator to a speed slightly below the limit slip (according to the set value Δf) by means of manual control. Excite the generator at the network voltage. The values can be read out under the operational measured values (address 5700) in the 7VE51.

Start the paralleling device. If a synchroscope is available, start at approx. synchronism "12 o'clock"; the duration up to the paralleling command then corresponds to exactly one cycle with the duration $1/\Delta f$ (i.e. 10 s at 0.1 Hz). Figure 6.16 shows an example. This attempt must be carried out several times for oversynchronous and subsynchronous switching provided each is permissible.

The dummy synchronization attempts can be repeated at the limits of the permissible voltage difference.

Correct functioning of the control commands must now be checked for devices with frequency and voltage balancing. The control command circuits must be made active again (reconnected); the close command remains disconnected. The control commands must be set to "Automatic".

Set the generator to a speed outside the off–control ranges. Start the paralleling device.

Check that the speed is influenced by the 7VE51 in the correct direction.

Warning

If the speed adjustment is not as envisaged, the device must be switched off immediately, manual mode must be selected, and the generator shut–down Correct the wiring of the control commands!

The command duration and the command pauses can be optimized if the direction of adjustment is correct (addresses 2⋆22 to 2⋆25, see Section 6.3.7).

(Dummy) paralleling attempts must be carried out both for overfrequency and underfrequency according to the parameterized values (addresses 2⋆07 and 2⋆08, Section 6.3.6).

Once the frequency balancing has been checked successfully, check the voltage balancing. Set the generator to approx. rated speed, but set the excitation to a voltage outside the permissible synchronization voltage. Start the paralleling device.

Check that the voltage is influenced by the 7VE51 in the correct direction.

Warning

If the voltage adjustment is not as envisaged, the device must be switched off immediately, manual mode must be selected, and the generator shut–down. Correct the wiring of the control commands!

The command duration and the command pauses can be optimized if the direction of adjustment is correct (addresses 2⋆27 to 2⋆30, see Section 6.3.8).

(Dummy) paralleling attempts must be carried out both for overvoltage and undervoltage according to the parameterized values (addresses 2⋆05 and 2⋆06, Section 6.3.6).

6.5.6 Operational paralleling

Stop the paralleling device (if not already done), switch the close command effective again.

The paralleling device is ready for use following positive termination of all checks and attempts. Check that the module(s) are inserted firmly and locked. The green LED "Service" must light up, the red LED "Blocked" must not light up.

Close the housing cover and tighten the screws. All terminal screws – including those which are not used – must be tightened firmly.

Finally carry out operational paralleling. It is best to start the 7VE51 when the phases are the same since paralleling is carried out the next time the phases have the same position providing the slip conditions remain unchanged.

Operational paralleling is described in detail in Section 6.6.

6.6 Paralleling procedure

When using to synchronize a generator, it is possible to set whether control commands are already output when the power supply is switched on or only when the device is started (see Section 6.3.7, address 2⋆17 for frequency balancing; Section 6.3.8, address 2⋆26 for voltage balancing). In the latter case, the device only becomes active following starting. The processor system runs−up after connection of the power supply. The device is ready after approx. 5 s. Following selection of the paralleling location, the device is informed via the associated binary input of which parameter block − and thus which set of setting values − is valid. The device is automatically blocked if no parameter block has been selected or if more than one block has been selected; the fault indication signals the blocked status. The device can now be started by exciting the binary input provided for this purpose. The start is stored even if a measured voltage is not yet present. The start signal must be present for at least 20 ms, however. A continuous signal is permissible. The device remains started until

- either a paralleling command is sent (up to the end of the command duration),
- or the parameterized active time (address 2⋆14) has expired,
- or the power supply is switched off,
- or a stop signal is applied via the binary input.

The stop signal must also be present for at least 20 ms. The stop signal has priority over the start signal, i.e. a start signal can have no effect as long as a stop signal is present. Renewed starting is possible following a stop.

If operational faults occur during starting, e.g. parameter selection faults, phase faults, measured voltage faults etc., the start is stopped immediately. The device can be started again once the fault has been eliminated.

Causes for reaction of the device to typical faults during paralleling attempts are listed in Section 6.6.4.

6.6.1 Paralleling of synchronous systems

The device carries out the following checks for the paralleling of synchronous systems:

- Are both measured voltages U1 and U2 within the permissible limits (addresses 2⋆01 and 2⋆02)?

- Do the phase sequences of the two voltages U1 and U2 correspond to the set phase rotation (addresses 2⋆03 and 2⋆04)?
  Note: Two phase−to−phase voltages must be connected for each measurement point in order to carry out a phase sequence check; the device blocks and signals this via the relay ”Device blocked” if the connection and the settings are contrary to one another or if the settings are non−plausible. ”Phase Seq. Flt.” appears in the operational annunciations (address 5100).

- Is the voltage difference ΔU within the permissible limits (addresses 2⋆05 and 2⋆06)?

- Is the frequency difference Δf within the permissible limits (address 2⋆36)? This should always be the case with synchronous systems.

- Is the angle difference $\Delta\varphi$ within the permissible limits (address 2⋆09)?

- Are the above−mentioned synchronization conditions satisfied for the complete set duration SYNCH. TIME (address 2⋆10)?

The close command is sent when the tests have been completed successfully. The duration of the close command has been set under address 2⋆13.

If not all synchronization conditions have yet been satisfied, the device continues to carry out the checks until the active time (address 2⋆14) has expired. The device then stops automatically.

6.6.2 Paralleling of asynchronous systems

The device monitors the following conditions following the start for the paralleling of asynchronous systems:

- Are both measured voltages U1 and U2 within the permissible limits (addresses 2⋆01 and 2⋆02)?
- Do the phase sequences of the two voltages U1 and U2 correspond to the set phase rotation (addresses 2⋆03 and 2⋆04)?
  Note: Two phase−to−phase voltages must be connected for each measurement point in order to carry out a phase sequence check; the device blocks and signals this via the relay "Device blocked" if the connection and the settings are contrary to one another or if the settings are non−plausible. "Phase Seq. Flt." appears in the operational annunciations (address 5100).
- Is the voltage difference ΔU within the permissible limits (address 2⋆05 and 2⋆06)?
- Is the frequency difference Δf within the permissible limits (addresses 2⋆07 and 2⋆08)?
- Is the angle difference of the two methods of measurement within the permissible angle window (address 2⋆11)?

Once the tests have been completed successfully, the device determines the next synchronization point from the change in angle and the frequency difference. The close command is output at a time which precedes the synchronization point by the closing time of the circuit breaker (address 2⋆12). The duration of the close command has been set under address 2⋆13.

The device carries out the checks until the close conditions have been satisfied, but at the longest for the active time (address 2⋆14). The device switches off automatically when paralleling has been successful or when the active time has expired.

6.6.3 Synchronization of generators

The device monitors the following conditions following the start for the synchronization of generators:

- Are both measured voltages U1 and U2 within the permissible limits (addresses 2⋆01 and 2⋆02)?
- Do the phase sequences of the two voltages U1 and U2 correspond to the set phase rotation (addresses 2⋆03 and 2⋆04)?
  Note: Two phase−to−phase voltages must be connected for each measurement point in order to carry out a phase sequence check; the device blocks and signals this via the relay "Device blocked" if the connection and the settings are contrary to one another or if the settings are non−plausible. "Phase Seq. Flt." appears in the operational annunciations (address 5100).
- Is the voltage difference ΔU within the permissible limits (address 2⋆05 and 2⋆06)?
- Is the frequency difference Δf within the permissible limits (addresses 2⋆07 and 2⋆08)?
- Is the angle difference of the two methods of measurement within the permissible angle window (address 2⋆11)?

If one or more of these conditions is not satisfied, the device outputs control commands provided it is equipped with the balancing functions (7VE512). **The control commands always have an effect on the voltage U2!** In the case of frequency deviations, these control commands are applied to the speed regulator whilst taking into consideration the parameters set in addresses 2⋆18 to 2⋆25. In the case of voltage deviations, the control commands are applied to the voltage regulator taking into consideration the parameters set in addresses 2⋆27 to 2⋆30.

The control commands can also already be output before starting the device if this is parameterized accordingly (address 2⋆17 for the frequency balancing and 2⋆26 for the voltage balancing).

The device monitors the reaction of the measured quantities to the control commands. If the paralleling conditions can be satisfied, the device determines the next synchronization point from the change in angle and the frequency difference. The close command is output at a time which precedes the synchronization point by the closing time of the circuit breaker (address 2⋆12). The duration of the close command has been set under address 2⋆13.

The device carries out the balancing and checks until the close conditions have been satisfied, but at the longest for the active time (address 2⋆14). The device switches off automatically when paralleling has been successful or when the active time has expired.

6.6.4 Reactions to faults during paralleling

The following tables list some reactions of the device to typical faults and errors during paralleling attempts:

Problem: Start command is not carried out

Possible fault of	Check:
Parameterizing	Circuit breaker closing time (address2⋆12) is still set to ∞; U MIN (address 2⋆01) is set greater than or equal to U MAX (address 2⋆02); Wrong off−control range: OS DEL fmin (address 2⋆19) is set greater than OS DEL fmax (address 2⋆18) or SS DEL fmin (address 2⋆21) is set greater than SS DEL fmax (address 2⋆20); Phase sequence settings (addresses 2⋆03 and/or 2⋆04) are not plausible (e.g. the one clockwise, the other counter−clockwise).
Initiation	More than one parameter set selected; No parameter set selected; Stop command is present; Parameter set selection is blocked after a synchronizing procedure.
Phase sequence	Voltage U_{L2-L3} is connected but U⋆ PH.SEQ. (address 2⋆03 or 2⋆04) is parameterized as *NONE* ; Wrong phase sequence (different to parameter addresses 2⋆03 and/or 2⋆04).
Measured voltages	Missing counter−phase voltage $\overline{U1}$ or $\overline{U2}$; Fault in instrument transformer circuit; Data error: U1 + $\overline{U1}$ or U2 + $\overline{U2}$ out of tolerance.
Hardware	Fault on basic module GEA; Fault on additional module ZEA (only 7VE512); Fault in command circuit; Fault in power supply.
Firmware	Check sum error recognized; Fault during processor system run−up.

Problem: Paralleling procedure is aborted:

Possible fault of	Check:
Initiation	Parameter set selection has been changed during operation; Missing parameter set selection; Stop signal received; Active time (address 2⋆14) expired.
Phase sequence	Missing voltage U_{L2-L3}; Phase sequence check disturbed.
Measured voltages	Measured voltage interruption after start; Fault in instrument transformer circuits; Data error: U1 + $\overline{U1}$ or U2 + $\overline{U2}$ out of tolerance.

Problem: Paralleling attempt unsuccessful:

Possible fault of	Check and correct:
Measured voltage(s) too high Measured voltage(s) too small	Read out voltage(s) in the operational measured values and compare with the set limit values
Frequency(ies) too high Frequency(ies) too small	Read out frequency(ies) in the operational measured values and compare with the operating range for paralleling
Frequency difference Δf out of operating range	Read out frequency difference in the operational measured values and compare with the operating range and the set limits; increase setting value for Δf (addresses 2⋆07 and/or 2⋆08) and/or ANGLE WINDW (address 2⋆11) if necessary
Frequency difference Δf varies around the limits between synchronous and asynchronous mode (10 mHz)	Only synchronous switching is allowed within a small angle range, as parameterized
Fluctuations in angle difference within the parameterized limit angle	This simulates asynchronism or Only synchronous switching is allowed, as parameterized

7 Maintenance and fault tracing

Siemens digital protection and automation devices are designed to require no special maintenance. All measurement and signal processing circuits are fully solid state and therefore completely maintenance free. Output relays are provided with protective covers.

As the device is almost completely self−monitored, from the measuring inputs to the command output relays, hardware and software faults are automatically annunciated. This ensures the high availability of the device and allows a more corrective rather than preventive maintenance strategy. Tests at short intervals become, therefore, superfluous.

With detected hardware faults the relay blocks itself; drop−off of the availability relay signals "equipment fault". If there is a fault detected in the external measuring circuits, generally an alarm is given only.

Recognized software faults cause the processor to reset and restart. If such a fault is not eliminated by restarting, further restarts are initiated. If the fault is still present after three restart attempts the protective system will switch itself out of service and indicate this condition by the red LED "Blocked" on the front plate. Drop−off of the availability relay signals "equipment fault".

The reaction to defects and indications given by the relay can be individually and in chronological sequence read off as operational annunciations under the address 5100, for defect diagnosis (refer to Section 6.4.2).

⚠ Warning

Ensure that the connection modules are not damaged when removing or inserting the device modules!

7.1 Routine checks

Routine checks of characteristics or pick−up values are not necessary as they form part of the continuously supervised firmware programs. The planned maintenance intervals for checking and maintenance of the plant can be used to perform operational testing of the equipment. The following procedure is recommended:

– Read−out of operational values (address block 57) and comparison with the actual values for checking the analog interfaces.

7.2 Fault tracing

If the paralleling device cannot be started, or a paralleling procedure in progress is aborted by the device, Section 6.6.4 will give you a survey of the probable causes.

If the device indicates a defect, the following procedure is suggested:

If none of the LEDs on the front plate of the module is on, then check:

– Have the modules been properly pushed−in and locked?

– Is the ON/OFF switch on the front plate in the ON position ⊙?

– Is the auxiliary voltage available with the correct polarity and of adequate magnitude, connected to the correct terminals (General diagrams in Appendix A)?

– Has the mini−fuse in the power supply section blown (see Figure 7.1)? If appropriate, replace the fuse according to Section 7.2.1.

If the red fault indicator "Blocked" on the front is on and the green ready LED remains dark, the device has recognized an internal fault. Re−initialization of the system could be tried by switching the d.c. auxiliary voltage off and on again. This, however, results in loss of fault data and messages and, if a parameterizing process has not yet been completed, the last parameters are not stored.

7.2.1 Replacing the mini−fuse

– Select a replacement fuse 5 × 20 mm. Ensure that the rated value, time lag (medium slow) and code letters are correct. (Figure 7.1).

– Prepare area of work: provide conductive surface for the basic module.

– Open housing cover.

Warning

Hazardous voltages can be present in the device even after disconnection of the supply voltage or after removal of the modules from the housing (storage capacitors)!

– Loosen the basic module using the pulling aids provided at the top and bottom. (Figure 7.2).

Caution!

Electrostatic discharges via the component connections, the PCB tracks or the connecting pins of the modules must be avoided under all circumstances by previously touching an earthed metal surface.

– Pull out basic module and place onto the conductive surface.

– Remove blown fuse from the holder (Figure 7.1).

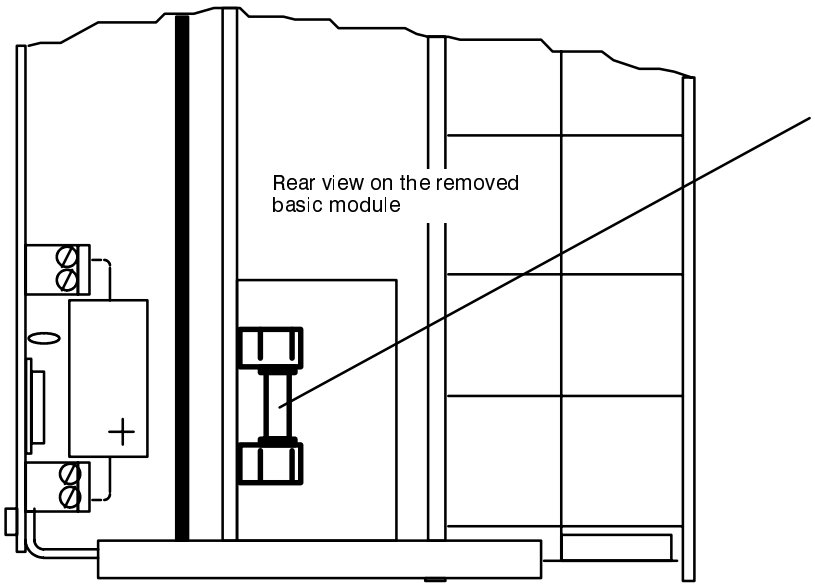
– Fit new fuse into the holder (Figure 7.1).

– Insert basic module into the housing; ensure that the releasing lever is pushed fully to the left before the module is pressed in (Figure 7.2).

– Firmly push in the module using the releasing lever. (Figure 7.2).

– Close housing cover.

Switch on the device again. If a power supply failure is still signalled, a fault or short−circuit is present in the internal power supply. The device should be returned to the factory (see Chapter 8).



at U_{HN}/V−	rated value
24/48	2 A/E
60/110/125	1,6 A/E
220/250	1 A/G

Figure 7.1 Mini−fuse of the power supply

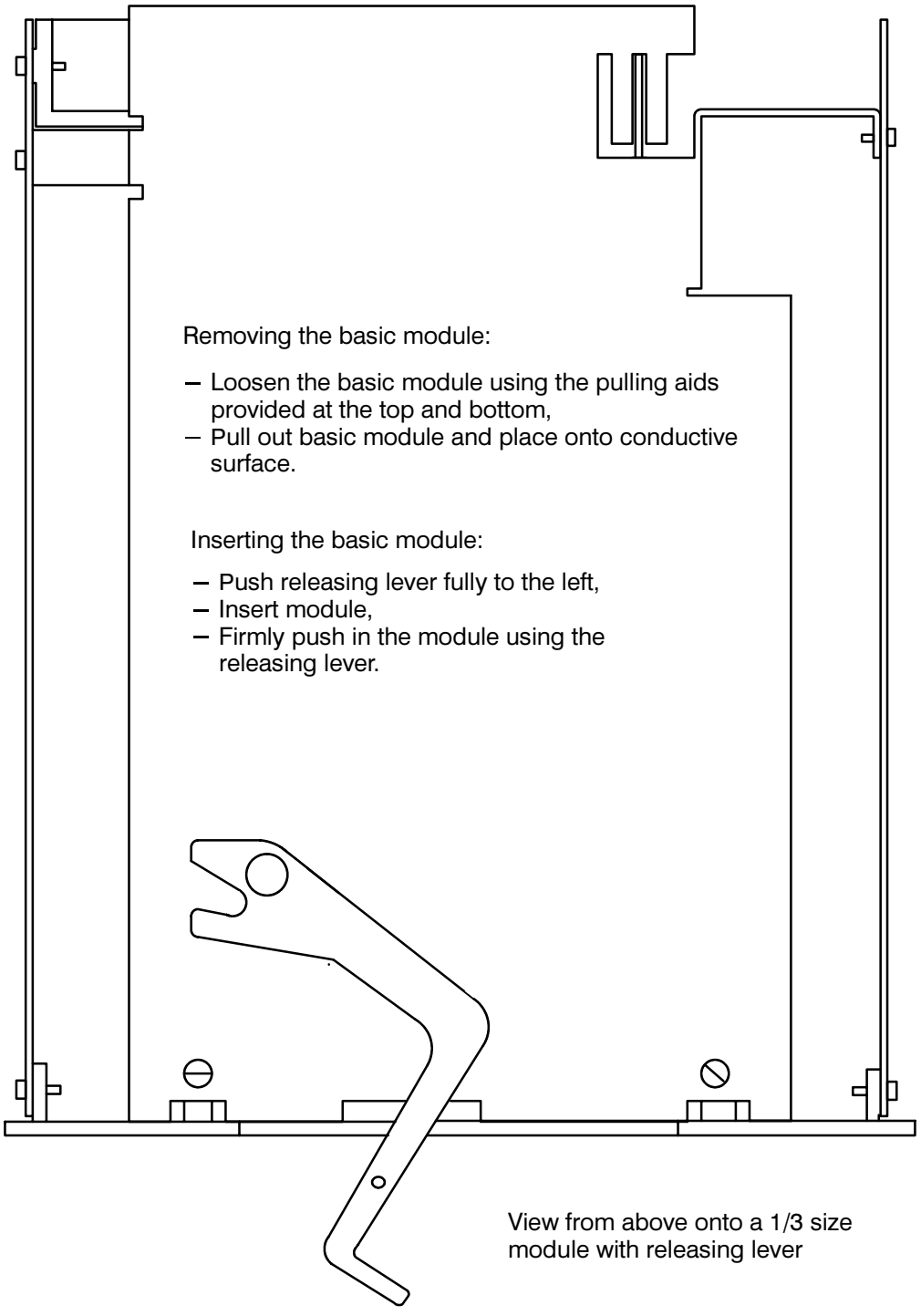


Figure 7.2 Aid for removing and inserting basic module

8 Repairs

Repair of defective modules is not recommended at all because specially selected electronic components are used which must be handled in accordance with the procedures required for **E**lectrostatically **E**ndangered **C**omponents (EEC). Furthermore, special manufacturing techniques are necessary for any work on the printed circuit boards in order to do not damage the bath−soldered multilayer boards, the sensitive components and the protective finish.

Therefore, if a defect cannot be corrected by operator procedures such as described in Chapter 7, it is recommended that the complete relay should be returned to the manufacturer. Use the original transport packaging for return. If alternative packing is used, this must provide the degree of protection against mechanical shock, as laid down in IEC 255−21−1 class 2 and IEC 255−21−2 class 1.

If it is unavoidable to replace individual modules, it is imperative that the standards related to the handling of **E**lectrostatically **E**ndangered **C**omponents are observed.

Warning

Hazardous voltages can be present in the device even after disconnection of the supply voltage or after removal of the module from the housing (storage capacitors)!

Caution!

Electrostatic discharges via the component connections, the PCB tracks or the connecting pins of the modules must be avoided under all circumstances by previously touching an earthed metal surface. This applies equally for the replacement of removable components, such as EPROM or EEPROM chips. For transport and returning of individual modules electrostatic protective packing material must be used.

Components and modules are not endangered as long as they are installed within the relay.

Should it become necessary to exchange any device or module, the complete parameter assignment should be repeated. Respective notes are contained in Chapter 5 and 6.

9 Storage

Solid state protective relays shall be stored in dry and clean rooms. The limit temperature range for storage of the relays or associated spare parts is −25 °C to +55 °C (refer Section 3.1.4 under the Technical data), corresponding to −12 °F to 130 °F.

The relative humidity must be within limits such that neither condensation nor ice forms.

It is recommended to reduce the storage temperature to the range +10 °C to +35 °C (50 °F to 95 °F); this prevents from early ageing of the electrolytic capacitors which are contained in the power supply.

For very long storage periods, it is recommended that the relay should be connected to the auxiliary voltage source for one or two days every other year, in order to regenerate the electrolytic capacitors. The same is valid before the relay is finally installed. In extreme climatic conditions (tropics) pre−warming would thus be achieved and condensation avoided.

Before initial energization with supply voltage, the relay shall be situated in the operating area for at least two hours in order to ensure temperature equalization and to avoid humidity influences and condensation.

Appendix

A General diagrams

B Connection diagrams

C Tables

A General diagrams

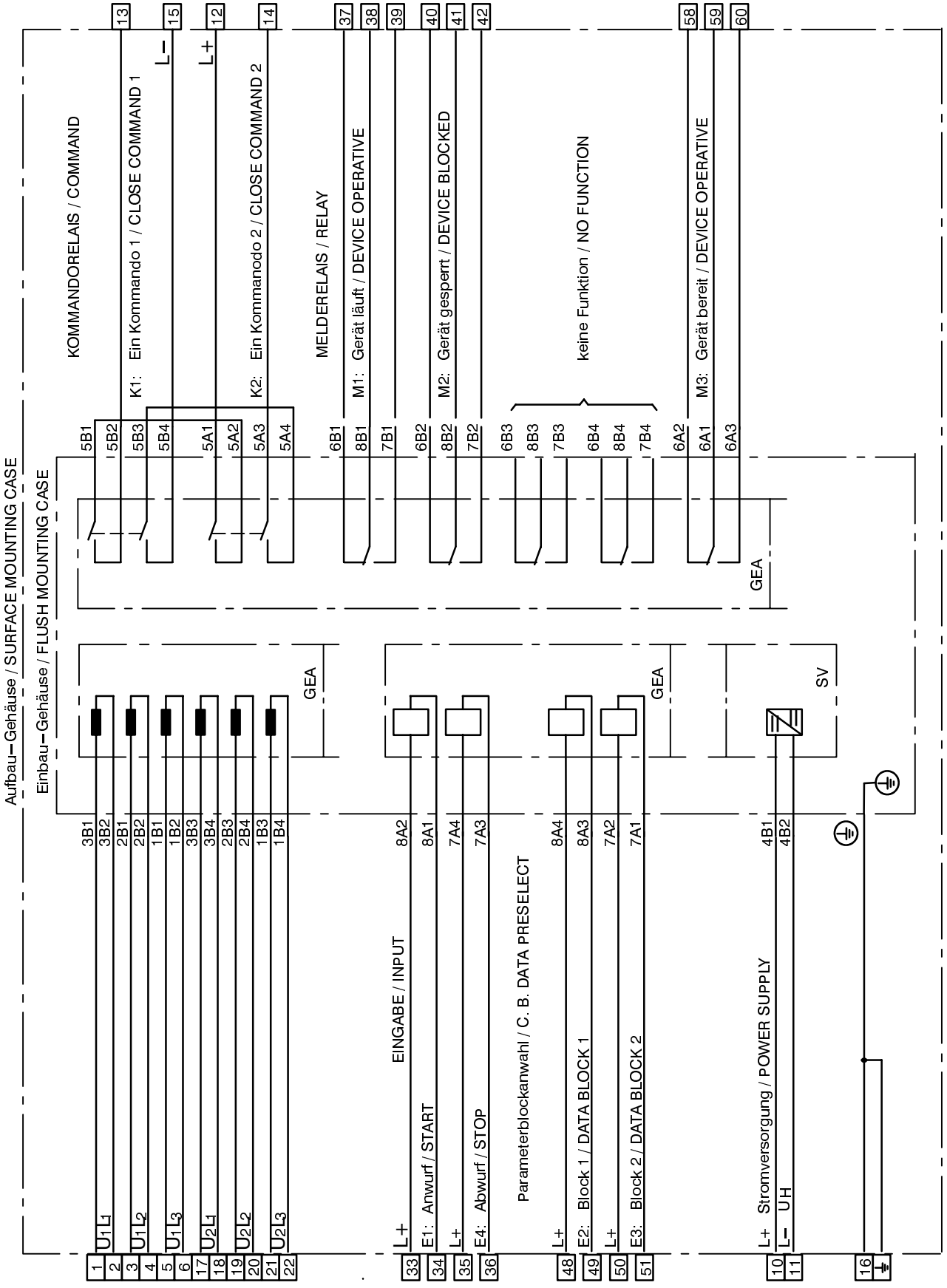


Figure A.1 General diagram of 7VE511

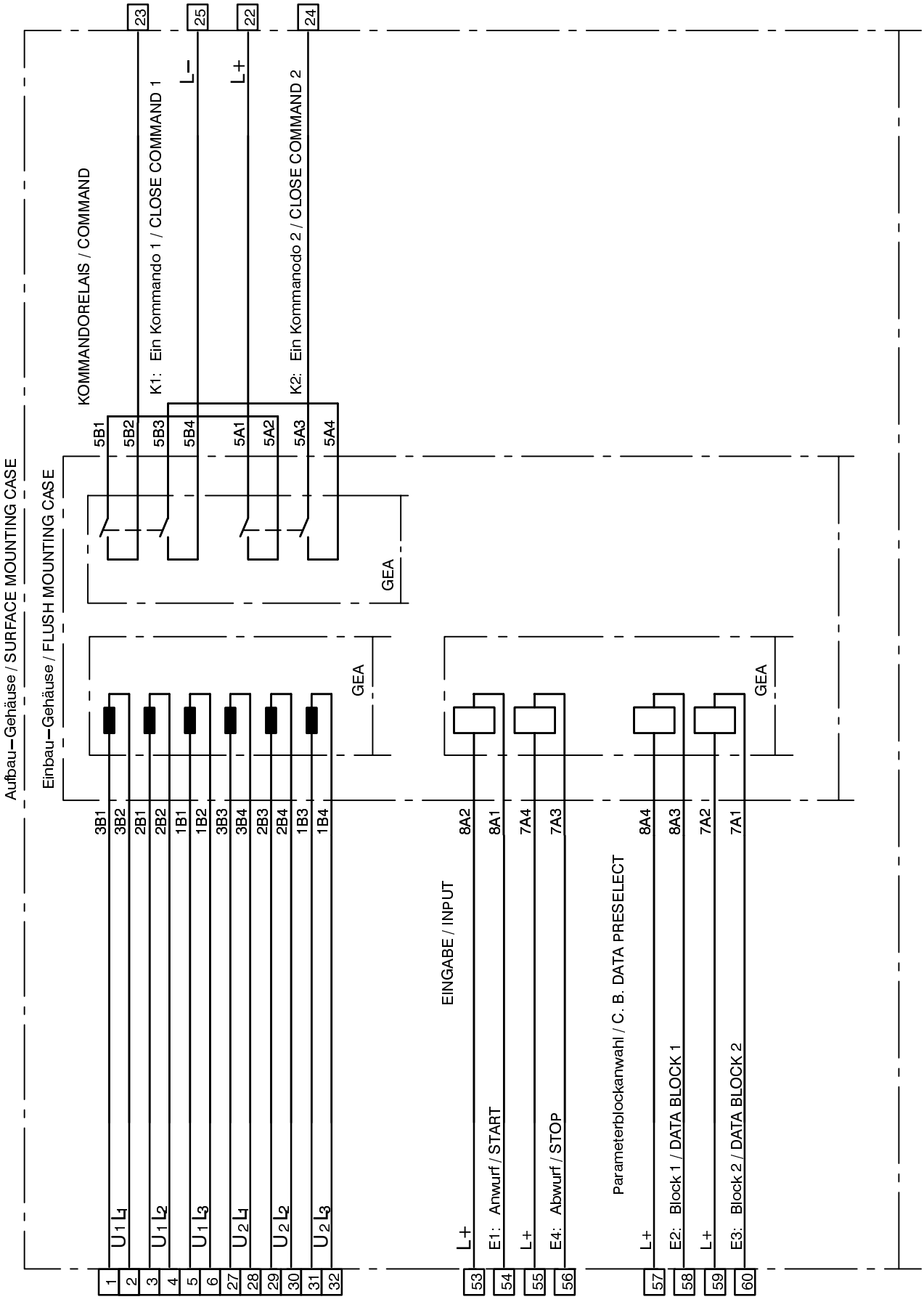


Figure A.2 General diagram of 7VE512 (sheet 1)

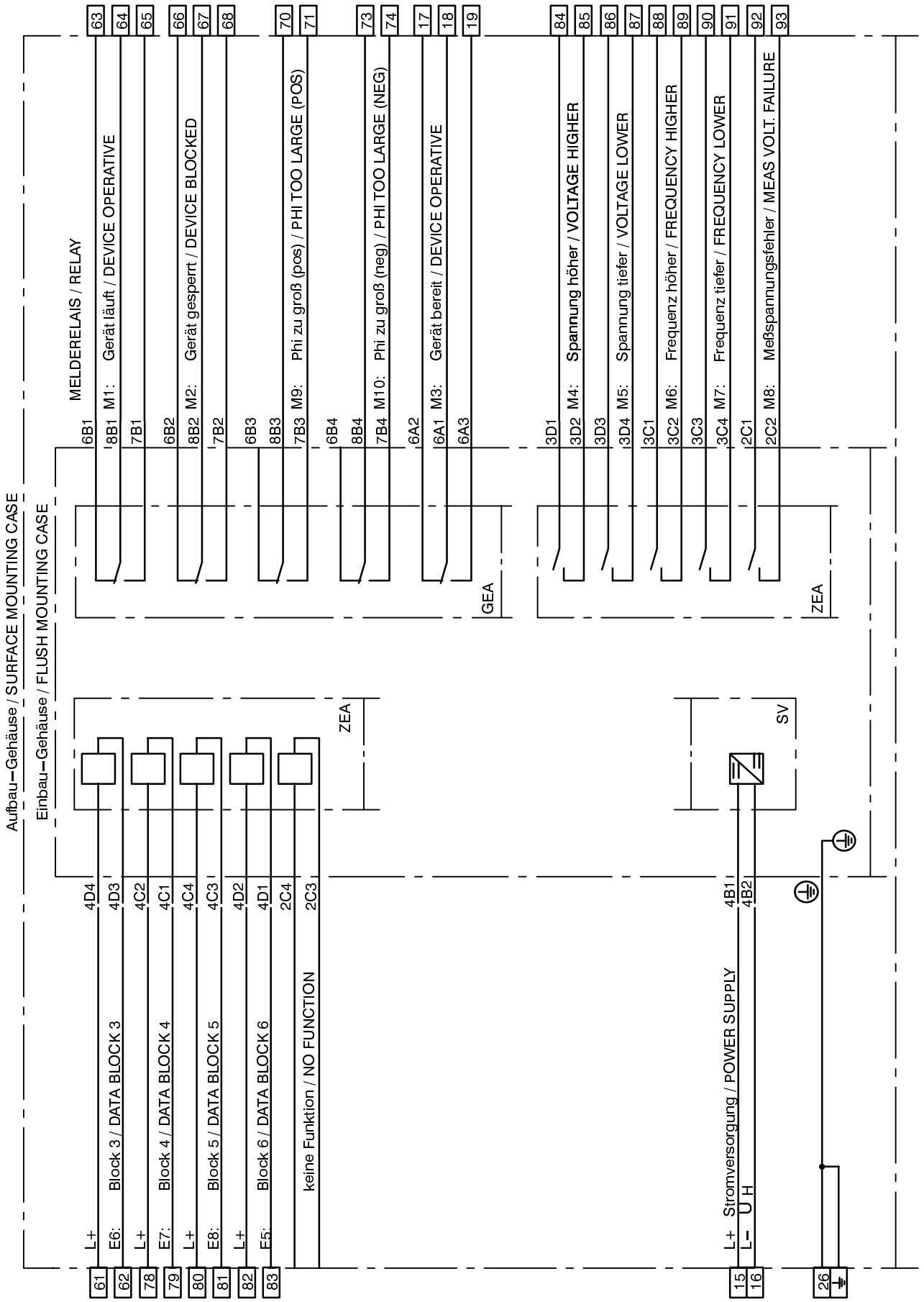


Figure A.3 General diagram of 7VE512 (sheet 2)

B Connection diagrams

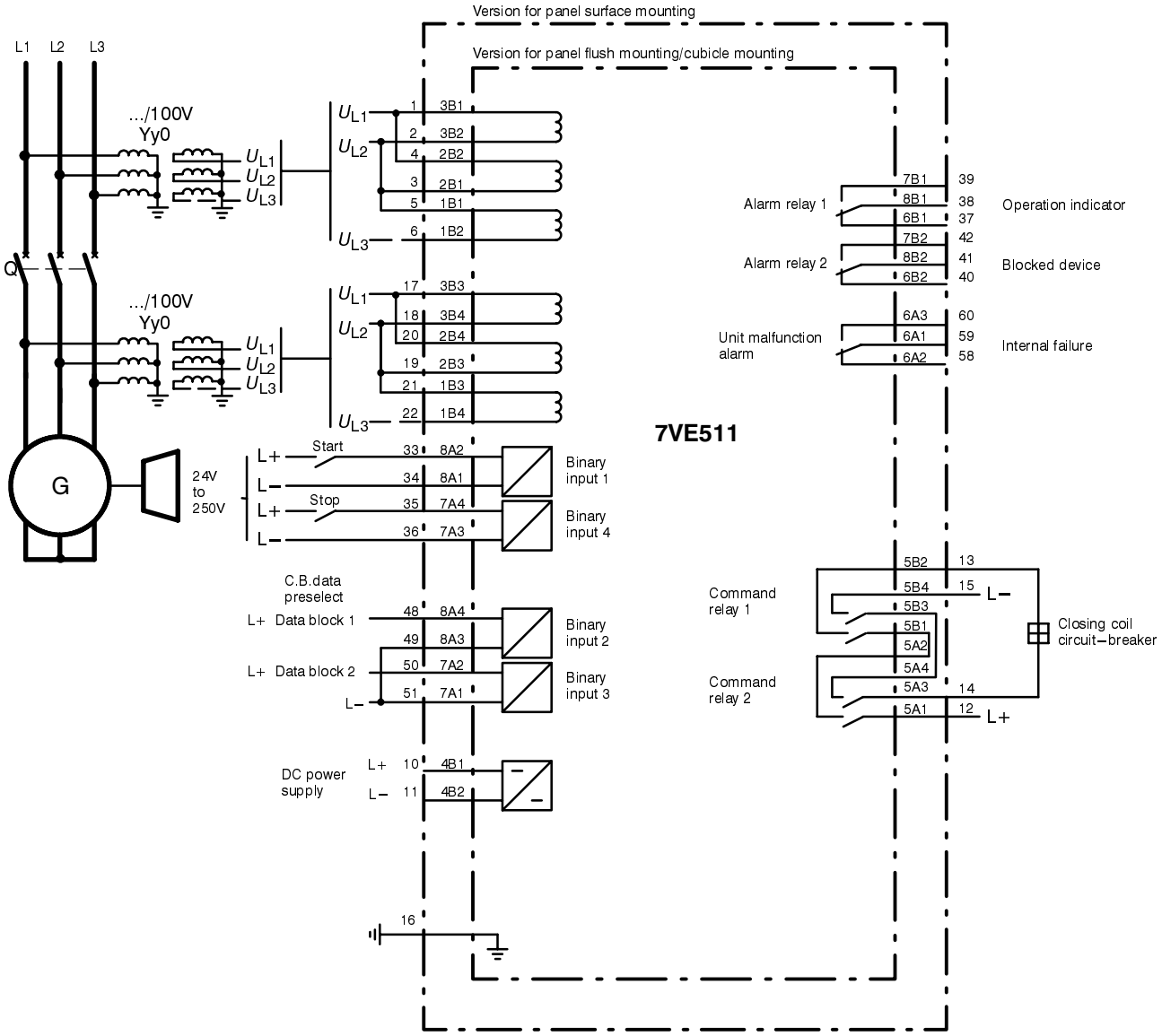


Figure B.1 Connection example 7VE511

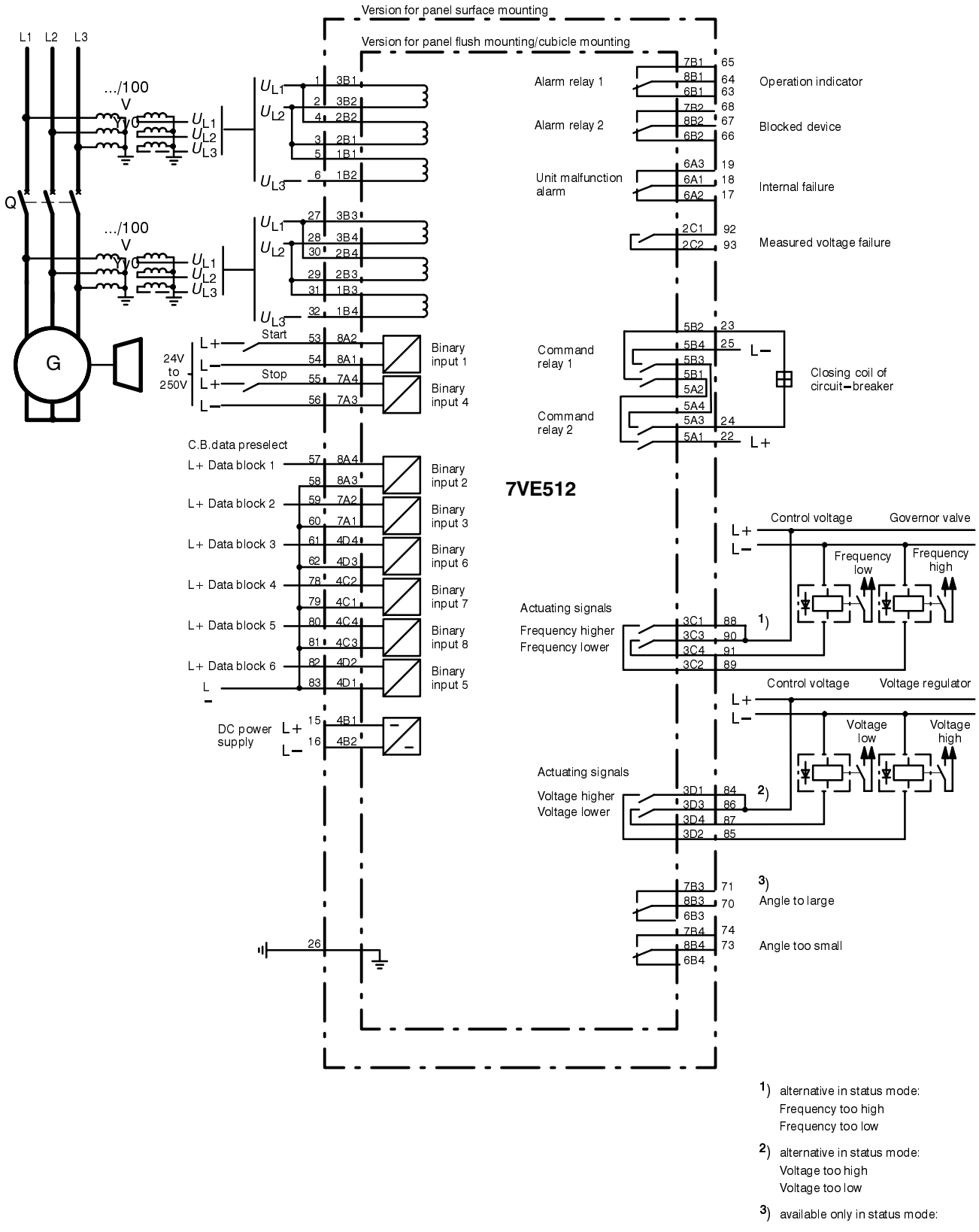


Figure B.2 Connection example 7VE512

Matching transformers

If there is another transformer between the voltage transformer of the generator feeder and the circuit breaker, e.g. of vector group Dy5, the vectors of the synchronizing voltages must be matched in magnitude and direction by means of matching transformers.

The circuit diagram B.5 is the circuit most commonly used, the circuit breaker S being controlled by the paralleling device.

In the other circuits shown below, the voltage vector is rotated according to the vector group of transformer T.

The ratings of the interposing transformers are as follows when the voltage transformer secondary side is rated for 100 V (110 V):

Designation 0 and 6: secondary voltage 100 V(110 V)
5 and 11: secondary voltage 100 V(110 V)/$\sqrt{3}$

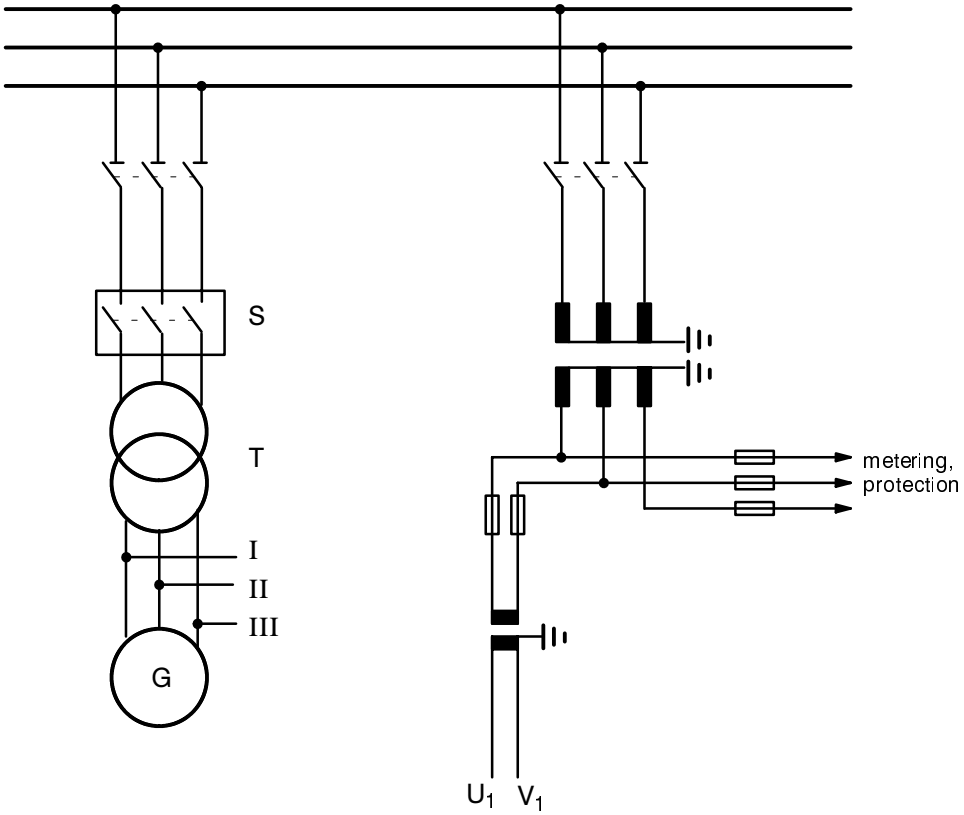


Figure B.3 Connection of matching transformers, e.g . for synchronization at the system side

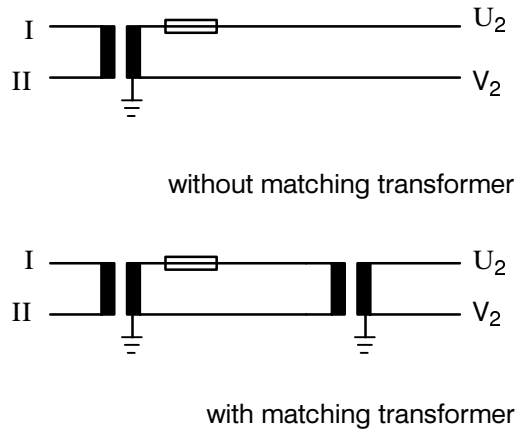
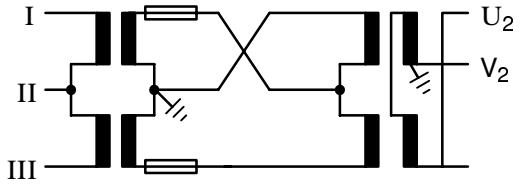
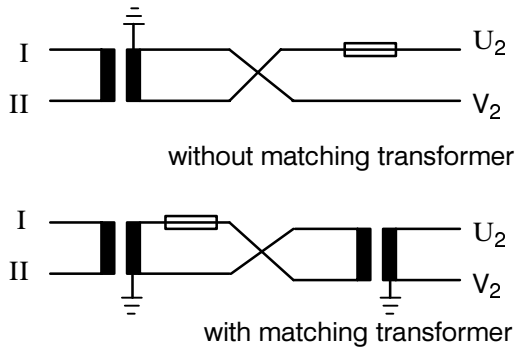
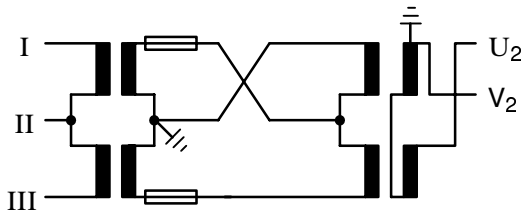
Numeral	Connection group	Voltage connection
0	Dd0 Yy0 Dz0	
5	Dy5 Yd5 Yz5	
6	Dd6 Yy6 Dz6	
11	Dy11 Yd11 Yz11	

Figure B.4 Connections of matching transformers

C Tables

NOTE: The following tables list all data which are available in the maximum complement of the device. Dependent on the ordered model, only those data may be present which are valid for the individual version.

NOTE: The actual tables are attached to the purchased relay.

Table of All Binary Outputs 7VE51

Rel,LED - to output relay or LED
OP, PC - to operator panel or PC
LSA - to localized substation autom.
R - Annunc. marshallable
K - Annunciated "Coming"
K/G - "Coming" and "Going"

FNo	Abbreviation	Meaning	Rel LED	OP PC	LSA
000					
002	SYNCHR.	Synchronization with consecutive No.		K/G	
030	LED-reset	Reset of stored LED indications		K	
031					
083	Failure 15V	Failure 15 V internal d.c. supply		K/G	
084	Failure 0V	Failure 0 V A/D converter		K/G	
088	Failure 24V	Failure 24 V internal d.c. supply		K/G	
089	Failure 5V	Failure 5 V internal d.c. supply		K/G	
091	Failure GEA	Failure on basic draw-out module		K/G	
092	Failure ZEA	Failure on additional draw-out module		K/G	
097	Par. running	Parameters are being set		K/G	
103	ParSelec.Flt	Faulty selection of a parameter set		K/G	
105	Par.Data Flt	Parameter data faulty (implausible)		K	
107	Initial.Flt	Faulty initialization of processor		K	
109	PhaseSeq.Flt	Phase sequence wrong		K/G	
110					
120	NO SET SELEC	No parameter set selected		K	
121	SET SELEC. 1	Parameter set 1 selected		K	
122	SET SELEC. 2	Parameter set 2 selected		K	
123	SET SELEC. 3	Parameter set 3 selected		K	
124	SET SELEC. 4	Parameter set 4 selected		K	
125	SET SELEC. 5	Parameter set 5 selected		K	
126	SET SELEC. 6	Parameter set 6 selected		K	
127					
192					
193	Re-start	Restart annunciation of the processor		K	
194					
195					
204	started:S1	Paralleling started with param. set 1		K	
205	started:S2	Paralleling started with param. set 2		K	
206	started:S3	Paralleling started with param. set 3		K	
207	started:S4	Paralleling started with param. set 4		K	
208	started:S5	Paralleling started with param. set 5		K	
209	started:S6	Paralelling started with param. set 6		K	
209	started	Paralleling procedure started		K	
210	aborted	Paralleling procedure aborted		K	
211	DeltaU ok	Delta U within the set limits		K	
212	DeltaU >>	Delta U too large		K	
213	DeltaF ok	Delta f within the set limits		K	
214	DeltaF >>	Delta f too large		K	

FNo	Abbreviation	Meaning	Rel LED	OP PC	LSA
215	Phi ok	Delta Phi within the set limits		K	
216	Phi >>	Delta Phi too large		K	
217	stopped	Paralleling stopped		K	
218	Tsyn over	Permissible synchronizing time over		K	
219	Close1 Cmd	Close command 1 (envelop curve method)		K	
221	Close2 Cmd	Close command 2 (zero crossing method)		K	
222	TsyncSTART	Time of synchronous condition started		K	
223	TsyncSTOP	Time of synchronous condition stopped		K	
224	Close1 res	Reset of close command 1		K	
225	close2 res	Reset of close command 2		K	
226	Fail.Umeas	Measured voltages faulty		K	
227	U1U2 synch	Voltages are synchronous		K	
228	U1U2 async	Voltages are asynchronous		K	
229	Sync.>1min	Synchron. condition greater than 1 min		K	
230					
231	F1 >>	Frequency f1 too large		K	
232	F1 <<	Frequency f1 too small		K	
233	F2 >>	Frequency f2 too large		K	
234	F2 <<	Frequency f2 too small		K	
235	U1 >>	Voltage U1 too large		K	
236	U1 <<	Voltage U1 too small		K	
237	U2 >>	Voltage U2 too large		K	
238	U2 <<	Voltage U2 too small		K	

Reference Table for Functional Parameters 7VE51

1000 PARAMETERS

1100 POWERSYSTEM DATA

1101 FREQUENCY
fN 50 Hz [ ]
fN 60 Hz [ ]

2100 PARAMETER SET 1

2101 U MIN
min. 40 V
max. 130 ———

2102 U MAX
min. 40 V
max. 130 ———

2103 U1 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2104 U2 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2105 DELTA U2>U1
min. 0.0 V
max. 30.0 ———

2106 DELTA U2<U1
min. 0.0 V
max. 30.0 ———

2107 DELTA f2>f1
min. 0.00 Hz
max. 1.01 ———

2108 DELTA f2<f1
min. 0.00 Hz
max. 1.01 ———

2109 DELTA PHI
min. 0 °
max. 45 ———

2110 SYNCH.TIME
min. 1 s
max. 60/∞ ———

2111 ANGLE WINDW
min. 2 °
max. 10 ———

2112 CB CLOSE TM
min. 30 ms
max. 600/∞ ———

```
2113 CMD. DURAT.
     min. 0.1                s
     max. 1.0       ———————

2114 ACTIVE TIME
     min. 1                  s
     max. 3600/∞    ———————

2117 FactorU2/U1
     min. 0.900
     max. 1.100     ———————

2135 SET BLOCK.
     ON                 [ ]
     OFF                [ ]

2136 DELTA f SYN
     min. 10                 mHz
     max. 40        ———————
```

```
2200 PARAMETER SET 2

2201 U MIN
     min. 40                 V
     max. 130       ———————

2202 U MAX
     min. 40                 V
     max. 130       ———————

2203 U1 PH.SEQ.
     CLOCKWISE          [ ]
     COUNTER-CLOCK      [ ]
     NONE               [ ]

2204 U2 PH.SEQ.
     CLOCKWISE          [ ]
     COUNTER-CLOCK      [ ]
     NONE               [ ]

2205 DELTA U2>U1
     min. 0.0                V
     max. 30.0      ———————

2206 DELTA U2<U1
     min. 0.0                V
     max. 30.0      ———————

2207 DELTA f2>f1
     min. 0.00               Hz
     max. 1.01      ———————

2208 DELTA f2<f1
     min. 0.00               Hz
     max. 1.01      ———————

2209 DELTA PHI
     min. 0                  °
     max. 45        ———————

2210 SYNCH.TIME
     min. 1                  s
     max. 60/∞      ———————

2211 ANGLE WINDW
     min. 2                  °
     max. 10        ———————

2212 CB CLOSE TM
     min. 30                 ms
     max. 600/∞     ———————

2213 CMD. DURAT.
     min. 0.1                s
     max. 1.0       ———————
```

```
2214 ACTIVE TIME
     min. 1                s
     max. 3600/∞   ———————

2217 FactorU2/U1
     min. 0.900
     max. 1.100    ———————

2235 SET BLOCK.
     ON                [ ]
     OFF               [ ]

2236 DELTA f SYN
     min. 10               mHz
     max. 40       ———————
```

```
2300 PARAMETER SET 1

2301 U MIN
     min. 40               V
     max. 130      ———————

2302 U MAX
     min. 40               V
     max. 130      ———————

2303 U1 PH.SEQ.
     CLOCKWISE         [ ]
     COUNTER-CLOCK     [ ]
     NONE              [ ]

2304 U2 PH.SEQ.
     CLOCKWISE         [ ]
     COUNTER-CLOCK     [ ]
     NONE              [ ]

2305 DELTA U2>U1
     min. 0.0              V
     max. 30.0     ———————

2306 DELTA U2<U1
     min. 0.0              V
     max. 30.0     ———————

2307 DELTA f2>f1
     min. 0.00             Hz
     max. 1.01     ———————

2308 DELTA f2<f1
     min. 0.00             Hz
     max. 1.01     ———————

2309 DELTA PHI
     min. 0                °
     max. 45       ———————

2310 SYNCH.TIME
     min. 1                s
     max. 60/∞     ———————

2311 ANGLE WINDW
     min. 2                °
     max. 10       ———————

2312 CB CLOSE TM
     min. 30               ms
     max. 600/∞    ———————

2313 CMD. DURAT.
     min. 0.1              s
     max. 1.0      ———————
```

```
2314 ACTIVE TIME
     min. 1                s
     max. 3600/∞   ———————

2317 FactorU2/U1
     min. 0.900
     max. 1.100    ———————

2318 FREQ.BALANC
     OFF              [ ]
     ON after start   [ ]
     ON before start  [ ]

2319 OS DEL fmax
     min. 0.01             Hz
     max. 1.00     ———————

2320 OS DEL fmin
     min. 0.01             Hz
     max. 1.00     ———————

2321 SS DEL fmax
     min. 0.01             Hz
     max. 1.00     ———————

2322 SS DEL fmin
     min. 0.01             Hz
     max. 1.00     ———————

2323 SS Kc
     min. 1
     max. 11       ———————

2324 SS Kp
     min. 1
     max. 10       ———————

2325 OS Kc
     min. 1
     max. 11       ———————

2326 OS Kp
     min. 1
     max. 10       ———————

2327 FB MIN PULS
     min. 30               ms
     max. 300      ———————

2328 VOLT.BALANC
     OFF              [ ]
     ON after start   [ ]
     ON before start  [ ]

2329 U2>U1 Kc
     min. 1
     max. 11       ———————

2330 U2>U1 Kp
     min. 1
     max. 10       ———————

2331 U2<U1 Kc
     min. 1
     max. 11       ———————

2332 U2<U1 Kp
     min. 1
     max. 10       ———————

2333 VB MIN PULS
     min. 30               ms
     max. 300      ———————

2335 SET BLOCK.
     ON                [ ]
     OFF               [ ]

2336 DELTA f SYN
     min. 10               mHz
     max. 40       ———————
```

2400 PARAMETER SET 2

2401 U MIN
min. 40 V
max. 130 _____

2402 U MAX
min. 40 V
max. 130 _____

2403 U1 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2404 U2 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2405 DELTA U2>U1
min. 0.0 V
max. 30.0 _____

2406 DELTA U2<U1
min. 0.0 V
max. 30.0 _____

2407 DELTA f2>f1
min. 0.00 Hz
max. 1.01 _____

2408 DELTA f2<f1
min. 0.00 Hz
max. 1.01 _____

2409 DELTA PHI
min. 0 °
max. 45 _____

2410 SYNCH.TIME
min. 1 s
max. 60/∞ _____

2411 ANGLE WINDW
min. 2 °
max. 10 _____

2412 CB CLOSE TM
min. 30 ms
max. 600/∞ _____

2413 CMD. DURAT.
min. 0.1 s
max. 1.0 _____

2414 ACTIVE TIME
min. 1 s
max. 3600/∞ _____

2417 FactorU2/U1
min. 0.900
max. 1.100 _____

2418 FREQ.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2419 OS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2420 OS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2421 SS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2422 SS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2423 SS Kc
min. 1
max. 11 _____

2424 SS Kp
min. 1
max. 10 _____

2425 OS Kc
min. 1
max. 11 _____

2426 OS Kp
min. 1
max. 10 _____

2427 FB MIN PULS
min. 30 ms
max. 300 _____

2428 VOLT.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2429 U2>U1 Kc
min. 1
max. 11 _____

2430 U2>U1 Kp
min. 1
max. 10 _____

2431 U2<U1 Kc
min. 1
max. 11 _____

2432 U2<U1 Kp
min. 1
max. 10 _____

2433 VB MIN PULS
min. 30 ms
max. 300 _____

2435 SET BLOCK.
ON [ ]
OFF [ ]

2436 DELTA f SYN
min. 10 mHz
max. 40 _____

2500 PARAMETER SET 3

2501 U MIN
min. 40 V
max. 130 _____

2502 U MAX
min. 40 V
max. 130 _____

2503 U1 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2504 U2 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2505 DELTA U2>U1
min. 0.0 V
max. 30.0 _____

2506 DELTA U2<U1
min. 0.0 V
max. 30.0 _____

2507 DELTA f2>f1
min. 0.00 Hz
max. 1.01 _____

2508 DELTA f2<f1
min. 0.00 Hz
max. 1.01 _____

2509 DELTA PHI
min. 0 °
max. 45 _____

2510 SYNCH.TIME
min. 1 s
max. 60/∞ _____

2511 ANGLE WINDW
min. 2 °
max. 10 _____

2512 CB CLOSE TM
min. 30 ms
max. 600/∞ _____

2513 CMD. DURAT.
min. 0.1 s
max. 1.0 _____

2514 ACTIVE TIME
min. 1 s
max. 3600/∞ _____

2517 FactorU2/U1
min. 0.900
max. 1.100 _____

2518 FREQ.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2519 OS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2520 OS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2521 SS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2522 SS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2523 SS Kc
min. 1
max. 11 _____

2524 SS Kp
min. 1
max. 10 _____

2525 OS Kc
min. 1
max. 11 _____

2526 OS Kp
min. 1
max. 10 _____

2527 FB MIN PULS
min. 30 ms
max. 300 _____

2528 VOLT.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2529 U2>U1 Kc
min. 1
max. 11 _____

2530 U2>U1 Kp
min. 1
max. 10 _____

2531 U2<U1 Kc
min. 1
max. 11 _____

2532 U2<U1 Kp
min. 1
max. 10 _____

2533 VB MIN PULS
min. 30 ms
max. 300 _____

2535 SET BLOCK.
ON [ ]
OFF [ ]

2536 DELTA f SYN
min. 10 mHz
max. 40 _____

2600 PARAMETER SET 4

2601 U MIN
min. 40 V
max. 130 _____

2602 U MAX
min. 40 V
max. 130 _____

2603 U1 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2604 U2 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2605 DELTA U2>U1
min. 0.0 V
max. 30.0 _____

2606 DELTA U2<U1
min. 0.0 V
max. 30.0 _____

2607 DELTA f2>f1
min. 0.00 Hz
max. 1.01 _____

2608 DELTA f2<f1
min. 0.00 Hz
max. 1.01 _____

2609 DELTA PHI
min. 0 °
max. 45 _____

2610 SYNCH.TIME
min. 1 s
max. 60/∞ _____

2611 ANGLE WINDW
min. 2 °
max. 10 _____

2612 CB CLOSE TM
min. 30 ms
max. 600/∞ _____

2613 CMD. DURAT.
min. 0.1 s
max. 1.0 _____

2614 ACTIVE TIME
min. 1 s
max. 3600/∞ _____

2617 FactorU2/U1
min. 0.900
max. 1.100 _____

2618 FREQ.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2619 OS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2620 OS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2621 SS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2622 SS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2623 SS Kc
min. 1
max. 11 _____

2624 SS Kp
min. 1
max. 10 _____

2625 OS Kc
min. 1
max. 11 _____

2626 OS Kp
min. 1
max. 10 _____

2627 FB MIN PULS
min. 30 ms
max. 300 _____

2628 VOLT.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2629 U2>U1 Kc
min. 1
max. 11 _____

```
2630 U2>U1 Kp
     min. 1
     max. 10       _______

2631 U2<U1 Kc
     min. 1
     max. 11       _______

2632 U2<U1 Kp
     min. 1
     max. 10       _______

2633 VB MIN PULS
     min. 30               ms
     max. 300      _______

2635 SET BLOCK.
     ON                [ ]
     OFF               [ ]

2636 DELTA f SYN
     min. 10               mHz
     max. 40       _______
```

```
2700 PARAMETER SET 5

2701 U MIN
     min. 40               V
     max. 130      _______

2702 U MAX
     min. 40               V
     max. 130      _______

2703 U1 PH.SEQ.
     CLOCKWISE         [ ]
     COUNTER-CLOCK     [ ]
     NONE              [ ]

2704 U2 PH.SEQ.
     CLOCKWISE         [ ]
     COUNTER-CLOCK     [ ]
     NONE              [ ]

2705 DELTA U2>U1
     min. 0.0              V
     max. 30.0     _______

2706 DELTA U2<U1
     min. 0.0              V
     max. 30.0     _______

2707 DELTA f2>f1
     min. 0.00             Hz
     max. 1.01     _______

2708 DELTA f2<f1
     min. 0.00             Hz
     max. 1.01     _______

2709 DELTA PHI
     min. 0                °
     max. 45       _______

2710 SYNCH.TIME
     min. 1                s
     max. 60/∞     _______

2711 ANGLE WINDW
     min. 2                °
     max. 10       _______

2712 CB CLOSE TM
     min. 30               ms
     max. 600/∞    _______

2713 CMD. DURAT.
     min. 0.1              s
     max. 1.0      _______
```

```
2714 ACTIVE TIME
     min. 1                s
     max. 3600/∞   ———————

2717 FactorU2/U1
     min. 0.900
     max. 1.100    ———————

2718 FREQ.BALANC
     OFF              [ ]
     ON after start   [ ]
     ON before start  [ ]

2719 OS DEL fmax
     min. 0.01             Hz
     max. 1.00     ———————

2720 OS DEL fmin
     min. 0.01             Hz
     max. 1.00     ———————

2721 SS DEL fmax
     min. 0.01             Hz
     max. 1.00     ———————

2722 SS DEL fmin
     min. 0.01             Hz
     max. 1.00     ———————

2723 SS Kc
     min. 1
     max. 11       ———————

2724 SS Kp
     min. 1
     max. 10       ———————

2725 OS Kc
     min. 1
     max. 11       ———————

2726 OS Kp
     min. 1
     max. 10       ———————

2727 FB MIN PULS
     min. 30               ms
     max. 300      ———————

2728 VOLT.BALANC
     OFF              [ ]
     ON after start   [ ]
     ON before start  [ ]

2729 U2>U1 Kc
     min. 1
     max. 11       ———————

2730 U2>U1 Kp
     min. 1
     max. 10       ———————

2731 U2<U1 Kc
     min. 1
     max. 11       ———————

2732 U2<U1 Kp
     min. 1
     max. 10       ———————

2733 VB MIN PULS
     min. 30               ms
     max. 300      ———————

2735 SET BLOCK.
     ON                [ ]
     OFF               [ ]

2736 DELTA f SYN
     min. 10               mHz
     max. 40       ———————
```

2800 PARAMETER SET 6

2801 U MIN
min. 40 V
max. 130 _____

2802 U MAX
min. 40 V
max. 130 _____

2803 U1 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2804 U2 PH.SEQ.
CLOCKWISE [ ]
COUNTER-CLOCK [ ]
NONE [ ]

2805 DELTA U2>U1
min. 0.0 V
max. 30.0 _____

2806 DELTA U2<U1
min. 0.0 V
max. 30.0 _____

2807 DELTA f2>f1
min. 0.00 Hz
max. 1.01 _____

2808 DELTA f2<f1
min. 0.00 Hz
max. 1.01 _____

2809 DELTA PHI
min. 0 °
max. 45 _____

2810 SYNCH.TIME
min. 1 s
max. 60/∞ _____

2811 ANGLE WINDW
min. 2 °
max. 10 _____

2812 CB CLOSE TM
min. 30 ms
max. 600/∞ _____

2813 CMD. DURAT.
min. 0.1 s
max. 1.0 _____

2814 ACTIVE TIME
min. 1 s
max. 3600/∞ _____

2817 FactorU2/U1
min. 0.900
max. 1.100 _____

2818 FREQ.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2819 OS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2820 OS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2821 SS DEL fmax
min. 0.01 Hz
max. 1.00 _____

2822 SS DEL fmin
min. 0.01 Hz
max. 1.00 _____

2823 SS Kc
min. 1
max. 11 _____

2824 SS Kp
min. 1
max. 10 _____

2825 OS Kc
min. 1
max. 11 _____

2826 OS Kp
min. 1
max. 10 _____

2827 FB MIN PULS
min. 30 ms
max. 300 _____

2828 VOLT.BALANC
OFF [ ]
ON after start [ ]
ON before start [ ]

2829 U2>U1 Kc
min. 1
max. 11 _____

```
2830 U2>U1 Kp
     min. 1
     max. 10       ______

2831 U2<U1 Kc
     min. 1
     max. 11       ______

2832 U2<U1 Kp
     min. 1
     max. 10       ______

2833 VB MIN PULS
     min. 30              ms
     max. 300      ______

2835 SET BLOCK.
     ON              [ ]
     OFF             [ ]

2836 DELTA f SYN
     min. 10              mHz
     max. 40       ______
```

To

SIEMENS AKTIENGESELLSCHAFT

Dept. EV S SUP 21

D–13623 BERLIN

Germany

From

_____
Name

_____
Company/Dept.

_____
Address

_____
Telephone no.

_____

Dear reader,

printing errors can never be entirely eliminated: therefore, should you come across any when reading this manual, kindly enter them in this form together with any comments or suggestions for improvement that you may have.

Corrections/Suggestions

Substantial alterations against previous issue:

Complete revision with regard to firmware version V1.7

Subject to technical alteration

Siemens Aktiengesellschaft

Order No. C53000–G1176–C80–7
Available from: LZF Fürth–Bislohe
Printed in the Federal Republic of Germany
AG 0199 0.3 FO 104 En